Roll No.												

PRESIDENCY UNIVERSITY

BENGALURU

Make Up Examinations – December 2025

Date: 26 – 12- 2025 **Time:** 1.00pm to 04.00pm

School: SOE	**Program:** B.TECH	
Course Code:ECE2002	**Course Name:** DIGITAL ELECTRONICS	
Semester: MK	**Max Marks**: 100	**Weightage**: 50%

CO - Levels	CO1	CO2	CO3	CO4	CO5
Marks	28	46	26	-	-

Instructions:

(i) Read all questions carefully and answer accordingly.

(ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks. **10Q x 2M=20M**

1.	State DeMorgan's Theorem for Two variables:	**2 Marks**	**L1**	**CO1**
2.	**A+B=B+A** for the given function, identify the name of Boolean law :	**2 Marks**	**L1**	**CO1**
3.	Write the name of the logic circuit which is used for logical addition(OR gate)	**2 Marks**	**L1**	**CO1**
4.	Find the correct value for **A+1=_____:**	**2 Marks**	**L1**	**CO1**
5.	Define Combinational Circuit:	**2 Marks**	**L1**	**CO2**
6.	Write the truth Table for Half Adder:	**2 Marks**	**L1**	**CO2**
7.	To Implement a Three variable Boolean function, how many number of 4X1 MUX(Multiplexers) needed?	**2 Marks**	**L1**	**CO2**
8.	Define Sequential Circuit:	**2 Marks**	**L1**	**CO3**
9.	Write the difference between Latch and Flip-flop	**2 Marks**	**L1**	**CO3**
10.	Write the characteristic equation for JK Flip-flop:	**2 Marks**	**L1**	**CO3**

Part B

Answer the Questions. **Total Marks 80M**

11.	**a.**	Find the minimum Boolean function and Implementing with basic and NAND logic gates. F(A,B,C,D)=∑(0,5,7,8,9,10,11,14,15)	**20 Marks**	**L2**	**CO1**
		Or			
12.	**a.**	Find the minimum Boolean function and Implementing with basic and NAND logic gates. F(A,B,C,D)=∑(0,2,3,6,7,8,10,12,13)	**20 Marks**	**L2**	**CO1**

13.	**a.**	Implement the given Boolean function using 8x1 MUX F(A,B,C,D)=∑(1,3,4,11,12,13,14,15)	**20 Marks**	**L3**	**CO2**
		Or			
14.	**a.**	Implement the given Boolean function using 8x1 MUX F(W X Y Z)=∑(0,2,3,6,8,9,13,14)	**20 Marks**	**L3**	**CO2**

15.	**a.**	Design the following Circuit: i) Half Adder using Basic logic gates ii) Full Adder using Basic Logic gate	**20 Marks**	**L3**	**CO2**
		Or			
16.	**a.**	Design the following Circuit: i) One bit Magnitude Comparator using Basic and NAND logic gates. ii)4x1 MUX using Basic gates	**20 Marks**	**L3**	**CO2**

17.	**a.**	State and Explain the following for JK Flip-flop: i) Circuit Diagram ii) State Table iii) State Equation/Next State Equation iv) Excitation Table	**15 Marks**	**L3**	**CO3**
	b.	Draw the SR latch circuit with enable input:	**5 Marks**	**L3**	**CO3**
		Or			
18.	**a.**	Design 3 bit UP counter using JK Flip-flop	**20 Marks**	**L3**	**CO3**