ROLL NO.	

PRESIDENCY UNIVERSITY, BENGALURU
SCHOOL OF ENGINEERING

Max Marks: 80 | Max Time: 180 Mins | Weightage: 40 %

ENDTERM FINAL EXAMINATION

I Semester AY 2017-18 | Course: **ECE/EEE 203 Digital Design** | 21 DEC 2017

Instructions:

i. Write legibly

ii. Scientific and nonprogrammable calculators are permitted

Part A

[5Q x 4M= 20 Marks]

1. State the difference between flip flop and latch.
2. Explain the Race around condition which occurs in J-K flip flop.
3. Explain the role of preset and clear in sequential circuits.
4. Discuss synchronous and asynchronous circuits with example for each.
5. Explain the working of Latch as a storage element shown in fig 1.1.

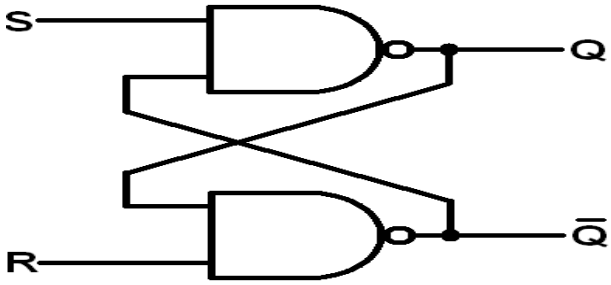

Fig 1.1

Part B

[3Q x 15M= 45 Marks]

6. Explain the working of bi -directional shit register. Discuss the right shift and left shift operation
7. Design 4 bit Ring counter and draw the timing diagram.
8. Design a S-R flip flop using T flip flop
   a. Design a characteristic table….
   b. Design a table of excitation for -----
   c. Design Boolean expression for the required flip-flop
   d. Draw the circuit diagram for required flip flop using

Part C

[1Q x 15M= 15Marks]

9. Design a 4 bit synchronous counter with D Flip Flop.

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Max Marks: 40 | Max Time: 60Min | Weightage: 20 %

TEST 2

I Semester AY 2017-2018 | Course: **ECE/EEE 203Digital Design** | 25 OCT 2017

Instructions:

i. Write legibly
ii. Scientific and non programmable calculators are permitted

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Part A

(3Q x 4 M= 12 Marks)

1. Design a combinational circuit which adds two binary numbers and produces sum and carry as output.
2. Implement the following Boolean function with active low output
   $f(x,y,z)= \sum(1,3,5,7)$
   $f(x,y,z)= \sum(2,4,6,7)$
3. Design a combinational circuit that compares two 1-bit input.
   .

Part B

(2Q x8 M= 16 Marks)

4. Explain difference between decoder and encoder. Explain the role of enable , Construct a 5-to-32 line decoder with four 3-to-8 line and one 2-to-4 line.
5. Design a n bit adder/substractor circuit and explain working with suitable example.

Part C

(1Q x 12 M= 12 Marks)

6. Design a combinational circuit that generates the 9's complement of BCD digits

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Max Marks: 40 | Max Time: 60Min | Weightage: 20 %

TEST 1

I Semester 2017-2018 | Course: **ECE/EEE 203 Digital Design** | 20 SEPT 2017

Instructions:

i. Write legibly
ii. Scientific and non programmable calculators are permitted

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Part A

(4Q x 3 M= 12 Marks)

1. Convert following numbers in respective form.
   a) $(396)_{10}=(\ )_2$ b) $(27)_8=(\ )_2$ c) $(110101)_2=(\ )_{10}$
2. Solve the following subtraction using 2's complement method.
   01100-00011
3. Solve the following expressions and simplify to minimum number of literal using Boolean rules.
   XY+X(WZ+WZ')
4. For the given logic diagram as shown in fig 1 which combination of input (A,B,C) makes output (y)=1
   Draw the truth table for the same.

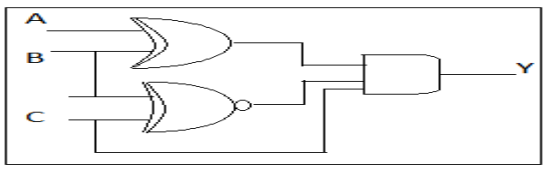

Fig 1

Part B

(2Q x8 M= 16 Marks)

5. Simplify the Boolean function into a)sum-of –products from b)product of sum form using K- map
   F(A,B,C,D)=∑m(0,1,2,5,8,9,10)

6. For the given function *f*= AB+AC'+C+AB'C+ABC
   a) Express f in standard SOP form
   b) Minimize it and realize the expression using basic gates .

Part C

(1Q x 12 M= 12 Marks)

7. For the Boolean function F= w'xy + wx'y + wxy

a) Obtain the truth table for the given expression

b) Draw the logic diagram using origin given expression.

c) Obtain the truth table of the function from the simplified expression and show that it is same

d) Draw the logic diagram from the simplified expression and compare the total number of gates with the diagram of part 7 (b).