ROLL NO.	

PRESIDENCY UNIVERSITY, BENGALURU
SCHOOL OF ENGINEERING

Max Marks: 80 | Max Time: 120 Mins | Weightage: 40 %

ENDTERM FINAL EXAMINATION

I Semester AY 2017-2018 | Course: **CSE 205 COMPUTER ORGANIZATION AND ARCHITECTURE** | 18 DEC 2017

Instructions:

i. Write legibly.

ii. No exchange of anything permitted.

Part A

[4 Q x 5 M= 20 Marks]

1. Explain cache *coherence*. State the solution.

2. Differentiate between *loosely coupled* and *tightly coupled* multiprocessing.

3. Explain *reliability* and *availability* of I/O devices. Give a measure of *availability*.

4. Derive a quantitative measure of pipelining speed-up. 'The gain in throughput from increasing the number of pipeline stages begins to diminish after a certain period'- justify the statement.

Part B

[2 Q x 15 M= 30 Marks]

5. i) Compare and contrast CISC and RISC architecture. **3**

ii) Explain *base-index-offset* and *memory-indirect* addressing modes with suitable instructions as examples in case of any RISC processor. **6**

iii) Write a recursive function to compute the factorial of 11, initially stored in register *r0*. Save the result in register *r1*. Use any RISC ISA. **6**

6. i) Explain the concept of virtual memory. **2**

ii) State how external fragmentation in memory can be reduced effectively. **2**

iii) 'Page size is always power of 2'-Explain. **2**

iv) Write the steps of handling a page fault in case of paging. **5**

v) Describe segmentation scheme in memory management. **4**

Part C

[2 Q x 15 M= 30 Marks]

7. i) Differentiate between polling and interrupt-driven I/O. **4**

ii) Explain Direct Memory Access. State what is '*stale data'* problem in DMA. Write the solutions for the same. **5**

iii) Explain the concept of RAID. Briefly describe the different RAID levels. State what is RAID 10. **6**

8. i) Explain the architecture of *superscalar* processors along with a neat block diagram and proper technical example. **4**

ii) State *Flynn's* classification of multiprocessors. Give proper examples of each class of multiprocessors. **5**

iii) Explain how *vector processors* function. Explain the vector instruction VectorSub.S Vi,Vj,Vk. **4+2**

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Max Marks: 40 | Max Time: 60 Mins | Weightage: 20 %

TEST 2

I Semester AY 2017-2018 Course: **CSE205 Computer Organization and Architecture** 27 OCT 2017

Instructions:

i. Write legibly.
ii. No exchange of anything permitted.

Part A

(3Q x 3 M= 09 Marks)

1. State the major stages of execution of an instruction. Distinguish between instruction cycle and machine cycle.

2. State what is Structural hazard in Instruction pipelining with example.

3. 'Pipelining does not reduce the execution time of an individual instruction, but increases instruction throughput'- Explain with example. Write an expression for pipeline speedup.

Part B

(2 Q x 8 M= 16 Marks)

4. 'Every processor state within a machine cycle is basically a RTL activity' – Explain. (2+6)
Describe the RTL activities done by the CPU during Instruction Fetch machine cycle with appropriate block diagram.

5. Design datapath and control path for the first CPU state of a typical Instruction Fetch machine cycle. (4+4)

Part C

(1 Q x 15 M= 15 Marks)

6. **A)** Explain what a 5 stage Instruction Pipeline is. 3
B) Differentiate *in-order* and *out-of-order* pipelines. 1
C) Describe the 3 types of Data hazards and their solutions. 5
D) State why only *forwarding* is not a solution for a Load-use data hazard. 3
E) Write what is Branch Prediction. State its necessity. 3

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CSE, SCHOOL OF ENGINEERING

Max Marks: 40 | Max Time: 60 Mins | Weightage: 20 %

TEST 1

V Semester 2017-2018 | Course: **CSE205 Computer Organization and Architecture** | 16 SEPT 2017

Instructions:

i. Write legibly.
ii. No exchange of anything permitted.

Part A

(3Q x 3 M= 09 Marks)

1. Describe the Von Neumann Architecture.
2. State the reasons why cache memory is generally made up of SRAM cells.
3. Explain memory hierarchy. Compare different types of memory using the three distinct memory comparison parameters.

Part B

(2 Q x 8 M= 16 Marks)

4. Explain the concept of virtual memory. Explain the locality of reference concept in detail. Explain what a Split cache is.
5. Explain the two distinct techniques of Cache writes. Also discuss their effects on system performance, precisely in handling cache misses.

Part C

(1 Q x 15 M= 15 Marks)

6. **A)** Assume a system cache of 4 one word blocks. The CPU needs to address the following sequence of main memory blocks : 5, 9, 5, 11, 9.
   Analyze and compare the Miss rates in each of the following cache mapping techniques.
   i) Direct Mapping
   ii) Fully Associative Mapping
   iii) 2-way Set Associative mapping. 9

   B) Explain the concept and advantages of memory interleaving with suitable examples. 6