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PRESIDENCY UNIVERSITY

BENGALURU

Mid - Term Examinations - March 2026

Date: 13- 03-2026

Time: 11.45am to 01.15pm

School: SOE	Program: B.Tech		
Course Code : ECE3039	Course Name: DSP Processors		
Semester: VI	Max Marks: 50	Weightage: 25%	

CO - Levels	C01	C02	C03	C04	C05
Marks	26	24			

Instructions:

- (i) Read all questions carefully and answer accordingly.
- (ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks.

5Q x 2M=10M

1	Find the DFT for unit impulse sequence?	2 Marks	L1	C01
2	How many complex multiplications are required for performing DFT with N point?	2 Marks	L1	C01
3	What are the computational building blocks of a processor?	2 Marks	L1	C01
4	What is the use of on-chip program memory of a DSP Processor?	2 Marks	L1	C02
5	For a sum of N numbers each of n bits, then what is the maximum number of bits to which sum can grow?	2 Marks	L1	C02

Part B

Answer the Questions.

Total Marks 40M

6.	a.	The discrete system is described by difference equation $y(n)=0.9y(n-1)+0.1x(n)$. Identify the type of digital filter, draw the corresponding block diagram and explain its features?	10 Marks	L2	CO1
	b.	Explain Basic DSP System with a block diagram and draw the waveforms of output of each block?	10 Marks	L2	CO1
Or					
7.	a.	Find the DFT for the sequence $x(n)=[2\ 3\ -1\ 4\ 2]$	10 Marks	L2	CO1
	b.	i) Convert 5.5 in to IEEE 754 single precision floating point number? ii) Convert following single precision binary number 0 1000001 0110000000000000000000 to decimal number	10 Marks	L2	CO1

8.	a.	What are basic DSP addressing modes? Explain with sample formats?	10 Marks	L2	CO2
	b.	Describe MAC unit with accumulator guard bits of a DSP Processor with a neat sketch?	10 Marks	L2	CO2
Or					
9.	a.	Illustrate and explain the memory space organization of the TMS320C54xx using a suitable memory map.	10 Marks	L2	CO2
	b.	Discuss the key architectural components and design features of the TMS320C54xx DSP.	10 Marks	L2	CO2