Roll No.												

PRESIDENCY UNIVERSITY

BENGALURU

Mid - Term Examinations – March 2026

Date: 11-03- 2026 **Time:** 11.45am to 01.15pm

School: SOE	**Program:** B.Tech	
Course Code : ECE3050	**Course Name**: Design for Testability	
Semester: VI	**Max Marks**: 50	**Weightage**: 25%

CO - Levels	CO1	CO2	CO3	CO4	CO5
Marks	26	24			

Instructions:

(i) Read all questions carefully and answer accordingly.

(ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks. **5Q x 2M=10M**

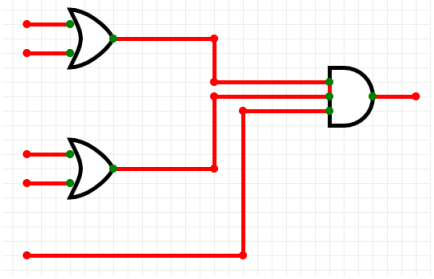
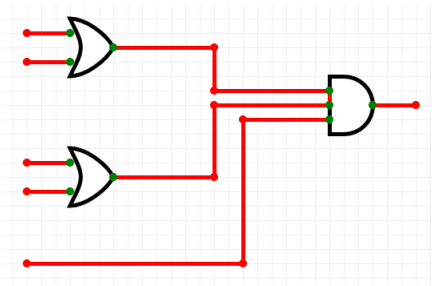
1	In general, topology-based testability analysis, such as SCOAP or probability-based testability analysis, is computationally efficient but can produce inaccurate results for circuits containing many reconvergent fanouts.What are the six numerical values available for a signal in a circuit for SCOAP analysis?	**2 Marks**	**L1**	**CO1**
2	To structurally test circuits, we need to control and observe logic values of internal lines. Level-sensitive scan design, also referred to as scan design, was the next, and most important, DFT technique What are the different scan cell design used in DFT?	**2 Marks**	**L1**	**CO1**
3	Suppose the system is in normal operation at t = 0, it fails at t1, and the normal system operation is recovered at t2 by some software modification, reset, or hardware replacement and if repair rate is 20. Then what is the value of MTTR?	**2 Marks**	**L1**	**CO1**
4	SCOAP was the first topology-based program that popularized testability analysis applications. Enhancements based on SCOAP have also been developed and used to aid in test point selection. Compute SCOAP and probability-based testability measures of a 3 input OR Gate?	**2 Marks**	**L1**	**CO2**
5	A delay fault causes excessive delay along a path such that the total propagation delay falls outside the specified limit. Delay faults have become more prevalent with decreasing feature sizes. What are different delay fault models?	**2 Marks**	**L1**	**CO2**

Part B

Answer the Questions. **Total Marks 40M**

6.	**a.**	At the switch level, a transistor can be stuck open or stuck short. These fault models cannot accurately reflect the behaviour of faults in CMOS logic circuits because of multiple transistors used. Illustrate the concept of above stuck faults in 2 input CMOS NAND gate with the help of truth table and explanation?	**10 Marks**	**L2**	**CO1**
	b.	The VLSI design process is essentially a process of transforming a higher level description of a design to a lower level description. Once verified, the VLSI design then goes to fabrication. Explain different levels of abstraction in VLSI design verification?	**10 Marks**	**L2**	**CO1**
		Or			
7.	**a.**	The number of failures in 10 power 9 hours is a unit (abbreviated FITS) that is often used in reliability calculations. There is a system with 200 components where each component has a failure rate of 1000 FITS, yield is 60% with fault coverage as 20% and system availability as 99.999%. Calculate the overall failure rate, MTBF, MTTR, repair rate, and defect level, for this system with necessary formulas?	**10 Marks**	**L2**	**CO1**
	b.	Bridging faults are those faults that involve a short between two signal lines in the digital circuit. The logic behaviour of a short defect between signal lines is commonly represented by the bridge fault model. Illustrate the concept of above faults with an example using truth table and explanation?	**10 Marks**	**L2**	**CO1**

8.	**a.**	Scan design attempts to ease the difficulty of testing by providing external access to selected storage elements in a design. This is accomplished by first converting selected storage elements in the design into scan cells and then stitching them together to form one or more shift registers, called scan chains. Explain about Clocked Scan Cell design and operation with suitable diagrams and waveforms?	**10 Marks**	**L2**	**CO2**
	b.	What are the SCOAP Combinational Controllability Calculation Rules for 1-Controllability (Primary Input, Output, Branch) of AND, OR, NOT gates. Calculate the SCOAP based Combinational Controllability and Observability measures for the following circuit?	**10 Marks**	**L2**	**CO2**

					
		Or			
9.	**a.**	In Scan architecture, all storage elements are replaced with scan cells, which are then configured as one or more shift registers (also called scan chains). Explain about Partial Scan circuit and test operation of scan architecture with neat sketches?	**10 Marks**	**L2**	**CO2**
	b.	What are the Probability based Controllability Calculation Rules for 1-Controllability (Primary Input, Output, Branch) of AND, OR, NOT gates. Calculate the Probability based Combinational Controllability and Observability measures for the following circuit? 	**10 Marks**	**L2**	**CO2**