Roll No.												

PRESIDENCY UNIVERSITY

BENGALURU

Mid - Term Examinations – MARCH 2026

Date: 10- 03- 2026 **Time:** 09:30am – 11:00am

School: SOE	**Program:** B .TECH	
Course Code: ECE3124	**Course Name:** VLSI DESIGN VERIFICATION	
Semester: VI	**Max Marks**: 50	**Weightage**: 25%

CO - Levels	**CO1**	**CO2**	**CO3**	**CO4**	**CO5**
Marks	**14**	**20**	**36**	**20**	**NA**

Instructions:

(i) Read all questions carefully and answer accordingly.

(ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks. **5Q x 2M=10M**

1	During simulation, output remains X. State one possible RTL-level cause.	**2 Marks**	**L2**	**CO3**
2	Differentiate between combinational and sequential circuits.	**2 Marks**	**L2**	**CO3**
3	Mention the difference between wire and reg data types in Verilog.	**2 Marks**	**L2**	**CO3**
4	A chip fails after fabrication due to an untested corner case. Classify whether this is a design, verification, or testing issue.	**2 Marks**	**L3**	**CO1**
5	A design team skips functional verification and directly proceeds to synthesis. Identify one major risk and one possible consequence.	**2 Marks**	**L3**	**CO1**

Part B

Answer the Questions. **Total Marks 40M**

6.	a.	Explain the complete Digital VLSI design flow from specification to fabrication. Clearly differentiate between design, verification, and testing.	10 Marks	L2	CO1
		Or			
7.	a.	Describe the role of verification versus testing in digital IC development. Explain why pre-silicon verification is critical.	10 Marks	L2	CO2
8.	a.	Design a testbench strategy to verify a 4-bit counter. Identify DUT, stimulus, and expected outputs.	10 Marks	L3	CO4
		Or			
9.	a.	Discuss the types of verification: functional, timing, and testing-oriented verification. Highlight their importance in modern VLSI systems.	10 Marks	L2	CO2
10.	a.	Given an RTL description containing both combinational and sequential logic, classify each block and justify your classification based on simulation behavior.	10 Marks	L3	CO4
		Or			
11.	a.	Given a 3:8 decoder combinational logic specification, develop the RTL logic, identify the appropriate always block, and explain the expected simulation waveform.	10 Marks	L3	CO3
12.	a.	Design a Moore state machine that outputs 1 whenever the binary input sequence “110” is detected (non-overlapping). a) Draw the state diagram b1) Write RTL code using always blocks	10 Marks	L3	CO3
		Or			
13.	a.	Design a Mealy state machine to detect the overlapping sequence “1011” from a serial input stream. a) Draw the state diagram b) Write the RTL (Verilog) code for the Mealy machine	10 Marks	L3	CO3