Roll No.												

PRESIDENCY UNIVERSITY

BENGALURU

Mid - Term Examinations – March 2026

Date: 12- 03- 2026 **Time:** 09:30am – 11.00am

School : SOE	**Program:** B TECH- VLSI	
Course Code: ECE3179	**Course Name:** Physical Design and Automation	
Semester: VI	**Max Marks**:50	**Weightage**:25%

CO - Levels	CO1	CO2	CO3	CO4	CO5
Marks	24	26			

Instructions:

(i) Read all questions carefully and answer accordingly.

(ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks. 5Q x 2M=10M

1	What is layout design?	**2 Marks**	**L1**	**CO1**
2	Define design rule checking (DRC)	**2 Marks**	**L1**	**CO1**
3	What are design rules?	**2 Marks**	**L1**	**CO2**
4	Define symbolic layout.	**2 Marks**	**L1**	**CO2**
5	List any two applications of layout compaction.	**2 Marks**	**L1**	**CO2**

Part B

Answer the Questions. Total Marks 40M

6.		VLSI design is carried out through a sequence of well-defined stages supported by EDA tools. With the help of a neat and well-labeled flow diagram, describe the complete VLSI design flow using EDA tools, starting from system specification and architectural design to physical design and final verification. Describe the objectives, inputs, and outputs of each design stage.	**10 Marks**	**L1**	**CO1**

		Or			
7.		Verification is a critical activity in ensuring the correctness and reliability of VLSI designs. Describe the various verification methods used in VLSI design automation, including functional, timing, and physical verification techniques. describe the role of each verification method at different abstraction levels.	**10 Marks**	**L1**	**CO1**
8.		Layout compaction plays a crucial role in optimizing VLSI physical design. With reference to this statement, explain the necessity of layout compaction in modern integrated circuit design.	**10 Marks**	**L2**	**CO2**
		Or			
9.		Partitioning is a fundamental step in handling large VLSI designs. In this context, analyze the working principle of the Kernighan–Lin (KL) partitioning algorithm, including initial partition formation, gain computation, node exchange strategy, and convergence behavior. Explain the effectiveness of the algorithm in minimizing cut size, and critically assess its advantages, limitations, and computational complexity when applied to large-scale circuits.	**10 Marks**	**L2**	**CO2**
10.		Describe the three major abstraction levels in VLSI design, namely structural design, logic design, and transistor-level design. For each level, describe the design objectives, representation techniques, constraints, and typical applications.	**10 Marks**	**L1**	**CO1**
		Or			
11.		The increasing complexity of modern VLSI systems has made design automation indispensable. The role of VLSI design automation tools in the context of algorithm development and system-level design. Describe how different algorithmic approaches are employed designs.	**10 Marks**	**L1**	**CO1**
12.		Constraint handling is a major challenge in VLSI layout optimization. Explain the formulation and application of constraint graph-based compaction algorithms, including the construction of horizontal and vertical constraint.	**10 Marks**	**L2**	**CO2**
		Or			
13.		Efficient partitioning algorithms are essential for optimizing large VLSI circuits. Explain the Fiduccia–Mattheyses (FM) partitioning algorithm, focusing on data structures used, gain computation strategy, pass-based optimization process, and stopping conditions. Explain how the FM algorithm improves partition quality	**10 Marks**	**L2**	**CO2**