Roll No.												

PRESIDENCY UNIVERSITY

BENGALURU

End Term Examinations – May/June 2026

Date: 14 – 05- 2026 **Time:** 09:30am – 12:30pm

School: SOIS	**Program:** BCA/BCD/BCI	
Course Code: CSA1201	**Course Name:** Computer Organization	
Semester: II	**Max Marks**: 100	**Weightage**: 50%

CO - Levels	CO1	CO2	CO3	CO4	CO5
Marks	26	24	24	26	

Instructions:

(i) Read all questions carefully and answer accordingly.

(ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks. **10Q x 2M=20M**

1.	List any 2 differences between uniprocessor and multiprocessor.	**2 Marks**	**L1**	**CO1**
2.	Elucidate different types of buses and their functions.	**2 Marks**	**L2**	**CO1**
3.	What is Power Wall?	**2 Marks**	**L1**	**CO1**
4.	Outline 4-bit ripple carry adder.	**2 Marks**	**L1**	**CO2**
5.	Apply 1's complement to evaluate $(8)_{10} - (2)_{10}$.	**2 Marks**	**L3**	**CO2**
6.	Tell the four stages of pipelining used in instruction execution in a computer architecture.	**2 Marks**	**L1**	**CO3**
7.	How does a multiplexer (MUX) function in datapath design?	**2 Marks**	**L1**	**CO3**
8.	A memory system uses 20 address lines. Calculate the maximum number of memory locations that can be addressed.	**2 Marks**	**L3**	**CO4**
9.	State any 2 differences between SRAM & DRAM.	**2 Marks**	**L1**	**CO4**
10.	Distinguish between Cache Hit & Cache Miss.	**2 Marks**	**L1**	**CO4**

Part B

Answer the Questions. **Total Marks 80M**

11.	**a.**	Explain the Functional Units of Computer with a suitable diagram and Find T (Total Time) by using following parameters: Consider there are 2000 instructions executing on 2Gz processor. The processor executes 30% instructions in 4 clock cycles, 50% in 5 clock cycles, remaining in 2 clock cycles.	**10 Marks**	**L2**	**CO1**
	b.	Register R3 and R4 of computer contain the decimal value 3500 and 2800 respectively. Determine addressing mode and effective address of the source/destination operand in each of the following instructions? (Assume 32bit word length) a) MOV 100(R3), R1 b) ADD 20(R3,R4), R2 c) STORE –(R3), R5 d) LOAD (R4)+, R6 e) ADD #250, R7	**10 Marks**	**L3**	**CO1**
		Or			
12.	**a.**	Elucidate below addressing modes with suitable syntax and example: a) Direct Addressing Mode b) Register Addressing Mode c) Implied Addressing Mode d) Auto Increment& Decrement Mode e) Base with Index and offset Addressing Mode	**10 Marks**	**L2**	**CO1**
	b.	Evaluate E=(A+B) * (C+D) using One, Two & Three Address instruction.	**10 Marks**	**L3**	**CO1**

13.	**a.**	Explain Big Endian and Little Endian. Determine Big Endian and Little Endian for the word "PYTHONIC" that stored in memory starting at address 2000. Assume that each character occupies 1 byte and 1 word = 4 bytes.	**10 Marks**	**L2**	**CO2**
	b.	Using the restoring division algorithm, compute the division of $(13)_{10}$ by $(3)_{10}$	**10 Marks**	**L3**	**CO2**
		Or			
14.	**a.**	Apply the 2's complement technique to perform the following arithmetic operations on signed binary numbers. (Assume 5bit binary representation) 1) (+4) − (+9) 2) (+2) + (+3) 3) (7) + (−5) 4) (−7) + (4) 5) (−8) + (−6)	**10 Marks**	**L2**	**CO2**

	b.	Apply Recoded Multiplier Booth algorithm on the given operands: $(13)_{10}*(-6)_{10}$ and explain the advantages achieved through recoding over conventional method.	**10 Marks**	**L3**	**CO2**

15.	**a.**	Explain building a datapath with a simple implementation scheme with a neat diagram.	**10 Marks**	**L2**	**CO3**
	b.	1) Consider the following instructions: I1: ADD R1, R2, R3 I2: SUB R4, R1, R5 I3: AND R6, R4, R7 I4: ADD R2, R3, R4 I5: MUL R5, R2, R6 Demonstrate data hazards in the above instructions.	**10 Marks**	**L3**	**CO3**
		Or			
16.	**a.**	Explain types of hazards with a suitable example.	**10 Marks**	**L2**	**CO3**
	b.	Illustrate the concept of pipelining and its advantages. Identify the type of data dependency and draw the pipeline execution diagram assuming a 5-stage pipeline (IF, ID, EX, MEM, WB) for the below instructions: I1: MUL R2, R3, R4 I2: ADD R5, R4, R6	**10 Marks**	**L3**	**CO3**

17.	**a.**	Explain Memory Hierarchy with a suitable diagram and discuss different types of memories.	**10 Marks**	**L2**	**CO4**
	b.	Suppose main memory consists of 32 blocks of 4 words each and cache consists of 4 blocks. Calculate bits required for main memory address? How many bits are there in each of Tag, block/set and word fields for different mapping techniques?	**10 Marks**	**L3**	**CO4**
		Or			
18.	**a.**	Summarize the three cache mapping techniques with appropriate diagrams.	**10 Marks**	**L2**	**CO4**
	b.	Demonstrate the following: 1) I/O Mapped I/O 2) Memory Mapped I/O 3) Interrupt-driven I/O communication	**10 Marks**	**L3**	**CO4**