Roll No.												

PRESIDENCY UNIVERSITY

BENGALURU

End - Term Examinations – May / June 2026

Date: 29- 05-2026 **Time:**09:30am – 12:30pm

School: SOE	**Program:** B. Tech. in ECE	
Course Code: ECE2501	**Course Name:** Linear Integrated Circuits	
Semester: IV	**Max Marks**: 100	**Weightage**: 50%

CO - Levels	CO1	CO2	CO3	CO4	CO5	CO6
Marks	24	24	14	14	12	12

Instructions:

(i) Read all questions carefully and answer accordingly.

(ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks. **10Q x 2M=20M**

1.	Describe the operation of a successive approximation type ADC. State how it determines the digital output for an analog input.	**2 Marks**	**L2**	**CO6**
2.	Compare the working of an inverting voltage comparator and a non-inverting voltage comparator. State how the output changes when the input exceeds the reference voltage in each case.	**2 Marks**	**L2**	**CO5**
3.	Describe the operation of a voltage-to-current converter with floating load. Write the expression for load current.	**2 Marks**	**L2**	**CO4**
4.	Explain the mathematical relationship between input and output for an op-amp integrator circuit. Write the output voltage expression.	**2 Marks**	**L2**	**CO4**
5.	Calculate the output voltage for an inverting amplifier with $R_1 = 1\ k\Omega$, $R_f = 2.2\ k\Omega$, and an input voltage $V_{in} = 2\ V$.	**2 Marks**	**L3**	**CO3**
6.	State the phase relationship between input and output for an inverting amplifier. Also, write the voltage gain expression.	**2 Marks**	**L1**	**CO3**

7.	Calculate the maximum output voltage at which the slew rate limit is reached for an op-amp with a slew rate of 0.5 V/μs when driven by a 100 kHz sine wave.	**2 Marks**	**L3**	**CO2**
8.	List the three open-loop configurations of an operational amplifier. In which configuration is the non-inverting terminal grounded?	**2 Marks**	**L1**	**CO2**
9.	Differentiate between input offset voltage (V_{io}) and input offset current (I_{io}) in an op-amp. Give typical values for IC 741.	**2 Marks**	**L2**	**CO1**
10.	Sketch the equivalent circuit of a *practical* operational amplifier and briefly explain why the input resistance is shown as a *large but finite* resistor and the output resistance as a *small but finite* resistor.	**2 Marks**	**L3**	**CO1**

Part B

Answer the Questions. **Total Marks 80M**

11.	**a.**	i) In an open-loop inverting amplifier using a 741 op-amp with $\boldsymbol{A = 4 \times 10^5}$ and supply voltages $\boldsymbol{V_{CC} = +15V, V_{EE} = -15V,}$ calculate the output voltage for: (A) $\boldsymbol{v_{in} = 30\,\mu V}$ (DC) (B) $\boldsymbol{v_{in} = 5\sin(2\pi \cdot 3000t)\,mV}$ ii) For case (B), sketch the input and output waveforms, indicating saturation limits.	**10 Marks**	**L3**	**CO1**
	b.	i) An op-amp has a differential gain $A_d = 1.5 \times 10^5$ and a common-mode gain $A_c = 0.04$. Calculate CMRR in dB. ii) If a differential input signal of 40 μV and a common-mode interference of 3 mV are applied simultaneously, find the output voltage. iii) What should be the maximum common-mode interference allowed if the error at the output due to common-mode signal should be less than 2% of the desired differential output?	**10 Marks**	**L3**	**CO1**
		Or			
12.	**a.**	i) A 741 op-amp has a slew rate of 0.8 $V/\mu s$. What is the maximum frequency of a 10 V peak-to-peak sine wave that can be amplified without slew-rate distortion? ii) If the same op-amp is used as a voltage follower with an input step of 12 V, calculate the rise time (10% to 90%) of the output. iii) If the input is a square wave of $\pm 8\,V$ at 50 kHz, will the output be distorted due to slew rate? Show calculations.	**10 Marks**	**L3**	**CO1**

	b.	i) The input bias current for a 741 op-amp is 800 nA and input offset current is 200 nA. Calculate the two input bias currents I_{B1} and I_{B2}. ii) If this op-amp is used in an inverting amplifier with $R_1 = 20\ k\Omega$ and $R_f = 200\ k\Omega$, and the non-inverting input is grounded through a resistor R_2, find the value of R_2 to minimize the output offset voltage due to bias currents. iii) Calculate the output offset voltage due to input offset current alone after compensation.	**10 Marks**	**L3**	**CO1**

13.	**a.**	You are required to design an inverting amplifier using an op-amp with the following specifications: • Desired closed-loop voltage gain: $\mathbf{A_V = -20}$ • Input resistance (seen from $\mathbf{v_{in}}$) should be $\mathbf{8\ k\Omega}$ • The op-amp is a 741C with $\mathbf{V_{CC} = +15V}$ and $\mathbf{V_{EE} = -15V}$ • Maximum expected input signal: $\mathbf{v_{in} = 0.6\ V}$ peak at $\mathbf{f = 2\ kHz}$ (i) Choose suitable standard resistor values for $\mathbf{R_1}$ and $\mathbf{R_f}$ to achieve the required gain while meeting the input resistance constraint. (ii) Calculate the output voltage expression for a sinusoidal input $\mathbf{v_{in}(t) = 0.6 sin(2\pi \times 2000t)}\ \boldsymbol{V}$, and determine its peak value.	**10 Marks**	**L3**	**CO2**
	b.	An inverting amplifier has $R_1 = 5.6\ k\Omega$ and $R_f = 33\ k\Omega$. For an input voltage of 2.0 V, calculate (i) voltage gain (A_V), (ii) output voltage (V_o), (iii) current through R_1 (I_1), (iv) current through R_f (I_f), and (v) input current (I_{in}).	**10 Marks**	**L3**	**CO2**
		Or			
14.	**a.**	(i) Design an inverting summing amplifier circuit to perform the following mathematical operation: $$V_o = -4V_1 - 6V_2$$ where V_1 and V_2 are DC input voltages. (ii) Sketch the complete circuit diagram of the inverting summing amplifier, labeling all components, inputs, outputs, and power supplies. (iii) Calculate the theoretical output voltage if $V_1 = 1.5$ V and $V_2 = 0.9$ V.	**10 Marks**	**L3**	**CO2**
	b.	Sketch the circuit of an inverting adder with two inputs and determine (derive) an expression for the output voltage.	**10 Marks**	**L3**	**CO2**

15.	**a.**	A non-inverting amplifier has $\boldsymbol{R_1 = 4.7\ k\Omega}$ and $\boldsymbol{R_f = 27\ k\Omega}$. For an input voltage of $\mathbf{1.8}\ \boldsymbol{V}$, calculate (i) voltage gain ($\boldsymbol{A_V}$), (ii) output voltage ($\boldsymbol{V_o}$), (iii) current through $\boldsymbol{R_1}$ ($\boldsymbol{I_1}$), (iv) current through $\boldsymbol{R_f}$ ($\boldsymbol{I_f}$), and (v) input current ($\boldsymbol{I_{in}}$).	**10 Marks**	**L3**	**CO3**

	b.	An op-amp integrator has $R = 20\,k\Omega$ and $C = 0.02\,\mu F$. The input is a square wave of $\pm 2\,V$ at $1\,kHz$. Calculate (i) the time constant RC, (ii) the rate of change of output voltage $\left(\frac{dv_o}{dt}\right)$ during the constant input period, and (iii) the peak-to-peak output voltage.	**10 Marks**	**L3**	**CO4**
		Or			
16.	**a.**	Design an inverting summing amplifier to perform $V_o = -6V_1 - 9V_2$ using $R_f = 18\,k\Omega$, and determine (i) R_1 and R_2, (ii) the output voltage when $V_1 = 0.5\,V$ and $V_2 = 0.3\,V$, and (iii) the current through R_f for the same inputs.	**10 Marks**	**L3**	**CO3**
	b.	An op-amp differentiator has $R = 15\,k\Omega$ and $C = 0.01\,\mu F$. The input is a triangular wave with peak-to-peak amplitude of $4\,V$ (from $-2\,V$ to $+2\,V$) at a frequency of $500\,Hz$. Calculate (i) the time constant RC, (ii) the rate of change of input voltage $\frac{dv_{in}}{dt}$, and (iii) the peak output voltage.	**10 Marks**	**L3**	**CO4**

17.	**a.**	Design a non-inverting Schmitt trigger for a lower threshold point of $\boldsymbol{-6\,V}$ and an upper threshold point of $\boldsymbol{+6\,V}$. Draw the circuit diagram, input waveform, output waveform, and transfer characteristics if the input is a $\boldsymbol{24\,V}$ peak-to-peak sine wave. Given $\boldsymbol{V_{CC} = 15\,V}$.	**10 Marks**	**L3**	**CO5**
	b.	Analyze the 3-bit Binary Weighted Resistors DAC and determine the output voltage for all 8 possible digital input combinations (from 000 to 111). Assume $V_{ref} = -8\,V$, $R_f = R$, and the op-amp is in inverting configuration. Calculate the output voltage for each case.	**10 Marks**	**L4**	**CO6**
		Or			
18.	**a.**	Design an inverting Schmitt trigger for a lower threshold point of $-5\,V$ and an upper threshold point of $+5\,V$. Draw the circuit diagram, input waveform, output waveform, and transfer characteristics if the input is a $20\,V$ peak-to-peak sine wave. Given $V_{CC} = 15\,V$.	**10 Marks**	**L3**	**CO5**
	b.	Analyze the 2-bit Binary Weighted Resistors DAC and determine the output voltage for all 4 possible digital input combinations (from 00 to 11). Assume $V_{ref} = -4\,V$, $R_f = R$, and the op-amp is in inverting configuration. Calculate the output voltage for each case.	**10 Marks**	**L4**	**CO6**