Roll No.												

PRESIDENCY UNIVERSITY

BENGALURU

End - Term Examinations – May / June 2026

Date: 27-05-2026 **Time:** 01:00pm – 04:00pm

School: SOE	**Program:** B.Tech	
Course Code: ECE3039	**Course Name:** DSP Processors	
Semester: VI	**Max Marks**: 100	**Weightage**: 50%

CO - Levels	CO1	CO2	CO3	CO4	CO5	CO6
Marks	14	14	14	24	24	10

Instructions:

(i) Read all questions carefully and answer accordingly.

(ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks. **10Q x 2M=20M**

1.	The Discrete Fourier Transform (DFT) converts a finite sequence of samples (time or spatial domain) into the same number of complex-valued frequency components. How many Real multiplications are required for N point DFT?	**2 Marks**	**L1**	**CO1**
2.	The Z-transform is a mathematical tool that converts discrete-time signals (sequences of numbers) into a complex frequency-domain representation, acting as the discrete-time equivalent of the Laplace transform. Find the Z transform of x(n)={2,0,-4,6,2,3}	**2 Marks**	**L1**	**CO1**
3.	On-chip memory refers to data storage (typically SRAM, ROM, or Flash) integrated directly onto the same silicon die as a processor or SoC (System-on-Chip). on-chip memory of TMS320C54XX can be extendable to?	**2 Marks**	**L1**	**CO2**
4.	Memory in Digital Signal Processors (DSPs) is optimized for high-speed, parallel access to data and instructions. Define DARAM?	**2 Marks**	**L1**	**CO2**

5.	What is the on-chip memory configuration if DROM of PMST Register is either 0 or 1?	**2 Marks**	**L1**	**CO3**
6.	PAGEN enhances performance by facilitating complex addressing modes like circular buffering. What is PAGEN?	**2 Marks**	**L1**	**CO3**
7.	For a sum of N numbers each of n bits, then what is the maximum number of bits to which sum can grow?	**2 Marks**	**L1**	**CO4**
8.	A Multiply-Accumulate (MAC) unit in a Digital Signal Processor (DSP) is a dedicated hardware block that multiplies two numbers and adds the product to an accumulator in a single cycle. Draw the flow chart for MAC unit?	**2 Marks**	**L1**	**CO4**
9.	Write the specification of CPU, Accumulator, multiplier and adder of TMS320C54XX ?	**2 Marks**	**L1**	**CO5**
10.	Circular addressing in DSP utilizes specialized hardware to automatically wrap address pointers around a defined buffer boundary (start/end). Write the formula for new ptr if SAR<EAR and updated ptr <EAR?	**2 Marks**	**L1**	**CO5**

Part B

Answer the Questions. **Total Marks 80M**

11.	**a.**	DSP (Digital Signal Processing) filters are algorithms or specialized hardware that mathematically manipulate sampled discrete-time signals to enhance or reduce specific frequency components. Explain FIR filter and IIR filter with equation, Block diagram and features?	**10 Marks**	**L2**	**CO1**
	b.	The Discrete Fourier Transform (DFT) converts a finite sequence of samples (time or spatial domain) into the same number of complex-valued frequency components. Find the DFT for the sequence x(n)=[2 4 -4 1 3]	**10 Marks**	**L3**	**CO2**
		Or			
12.	**a.**	Precision in Digital Signal Processing (DSP) refers to the number of bits used to represent numerical values, determining the resolution and accuracy of signals. i) Convert 9.125 in to IEEE 754 single precision floating point number? ii) Convert following single precision binary number 0 10000011 00100100000000000000000 to decimal number	**10 Marks**	**L2**	**CO1**
	b.	The Fast Fourier Transform (FFT) is an efficient algorithm that computes the Discrete Fourier Transform (DFT), converting	**10 Marks**	**L3**	**CO2**

		signals from the time/space domain to the frequency domain. Find the FFT for the sequence x(n)=[8 2 6 -1 3]			

13.	**a.**	The Address Generation Unit (AGU) in a Digital Signal Processor (DSP) is a dedicated hardware module that calculates memory addresses in parallel with data processing, typically enabling one or more address computations per clock cycle. Explain Address generation unit with a neat sketch?	**10 Marks**	**L2**	**CO3**
	b.	Digital Signal Processor (DSP) is a specialized microprocessor designed to perform high-speed mathematical operations on digitized real-world signals. Explain the features of Programmable DSP Processor?	**10 Marks**	**L3**	**CO4**
		Or			
14.	**a.**	TMS DSP processors are dominant family of high-performance Digital Signal Processors (DSPs) and DSP controllers designed for real-time processing, introduced in 1983. Discuss the key architectural components and design features of the TMS320C54xx DSP using neat sketch.	**10 Marks**	**L2**	**CO3**
	b.	Illustrate and explain the memory space organization of the TMS320C54xx using a suitable memory map.	**10 Marks**	**L3**	**CO4**

15.	**a.**	Addressing modes in Digital Signal Processors (DSPs) are specialized techniques for accessing operands (data) from memory to be processed by the CPU, designed to speed up operations like convolutions, Fast Fourier Transforms (FFT), and filtering. Explain Circular addressing mode with an example and neat sketch?	**10 Marks**	**L2**	**CO4**
	b.	Programming DSP (Digital Signal Processor) chips involves creating high-speed, mathematical algorithms for real-time signal analysis. Write an ALP for computing the sum of 3 product terms given by equation Y(n)=h0x(n)+h1x(n-1)+h2x(n-2)+h3x(n-3)	**10 Marks**	**L3**	**CO5**
		Or			
16.	**a.**	The TMS320C54xx is a family of fixed-point digital signal processors (DSPs) from Texas Instruments designed for high-performance, low-power applications . Explain TMS320C54XX addressing modes with examples?	**10 Marks**	**L2**	**CO4**
	b.	Write an ALP for sum of series of positive numbers stored at successive memory locations in data memory and place the result in memory location?	**10 Marks**	**L3**	**CO5**

17.	**a.**	Represent the following fixed point 16 bit number 6000H in Q15, Q7, Q9 and find its decimal equivalent? Write an ALP for multiplying a sequence with a scalar value?	**10 Marks**	**L3**	**CO5**
	b.	Interfacing with DSP processors involves connecting external components like ADCs and DACs to process real-time analog signals in the digital domain Explain Interrupts and I/O interface with neat sketch and timing diagram?	**10 Marks**	**L2**	**CO6**
Or					
18.	**a.**	Represent the following fixed point 16 bit decimal number 4.125 in Q15, Q7, Q9? Write an ALP for square of a signal?	**10 Marks**	**L3**	**CO5**
	b.	Programmed I/O (PIO) in Digital Signal Processing (DSP) is a data transfer method where the CPU directly controls input/output operations, continuously polling device status registers to check for readiness. Explain Programmed I/O interface with neat sketch and timing diagram?	**10 Marks**	**L2**	**CO6**