Roll No.												

PRESIDENCY UNIVERSITY

BENGALURU

End - Term Examinations – May / June 2026

Date: 20- 05-2026 **Time:**01:00pm – 04:00pm

School: SOE	**Program**: B.Tech	
Course Code: ECE3050	**Course Name:** Design for Testability (DFT)	
Semester: VI	**Max Marks**: 100	**Weightage**: 50%

CO - Levels	CO1	CO2	CO3	CO4	CO5	CO6
Marks	20	16	16	8	20	20

Instructions:

(i) Read all questions carefully and answer accordingly.

(ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks. **10Q x 2M=20M**

1.	Probability-based controllability extends traditional system control theory by accounting for stochastic behaviors, component failures, or uncertain environmental conditions. What is the boundary condition for controllability and observability based on Probability approach?	**2 Marks**	**L1**	**CO2**
2.	Scan architecture is a Design for Testability (DFT) technique that converts internal sequential elements (flip-flops) into a shift registes. What are different IOs in scan architecture?	**2 Marks**	**L1**	**CO3**
3.	SCOAP (Sandia Controllability & Observability Analysis Program) is a testability analysis technique in Design for Testability (DFT) that quantifies how easy or hard it is to control and observe internal digital circuit nodes. Compute SCOAP and probability-based testability measures of a 3 input AND Gate?	**2 Marks**	**L1**	**CO2**
4.	High controllability simplifies testing, reducing the need for extensive test vectors and increasing fault coverage Define controllability?	**2 Marks**	**L1**	**CO2**

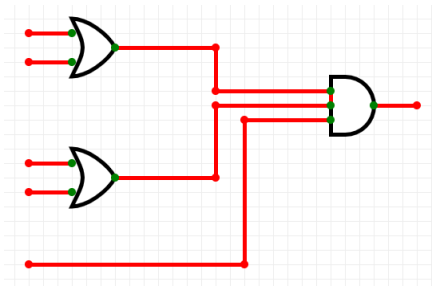
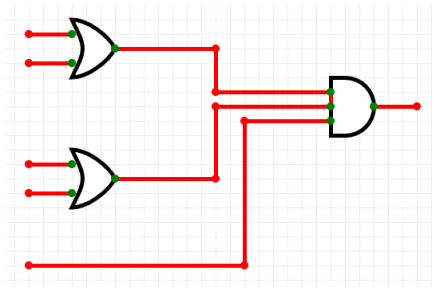
5.	A scan cell in Design-for-Test (DFT) is a modified flip-flop (typically a Muxed-D type) that replaces standard flops to enhance controllability and observability. Draw a neat sketch of Muxed D scan cell?	**2 Marks**	**L1**	**CO3**
6.	Scan cell primarily refers to a specialized VLSI flip-flop used in circuit testing. What are different scan cell designs?	**2 Marks**	**L1**	**CO3**
7.	Faults often causing devices to stop working, overheat, or enter protect mode. Common causes include thermal overstress, excessive voltage/current, or physical damage. Define open and short faults?	**2 Marks**	**L1**	**CO4**
8.	For a circuit of n fault sites and k types of faults, how many single faults will be present?	**2 Marks**	**L1**	**CO4**
9.	Defect levels define the quality threshold of products, typically measured as the percentage of faulty items or defects per million (DPM). Write the equation for defect level?	**2 Marks**	**L1**	**CO4**
10.	Faults in Design for Testability (DFT) are logical representations of physical manufacturing defects, Define bridging fault?	**2 Marks**	**L1**	**CO4**

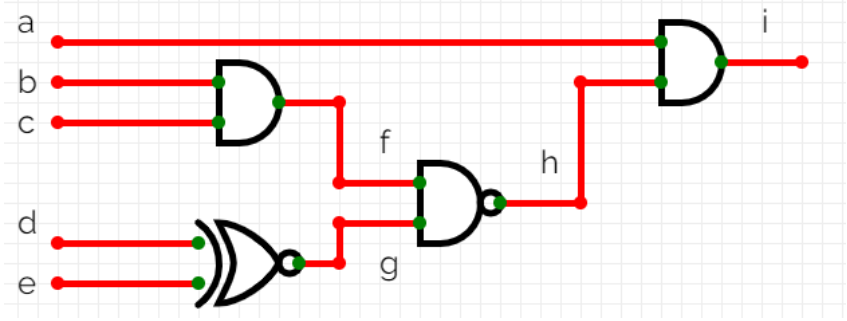
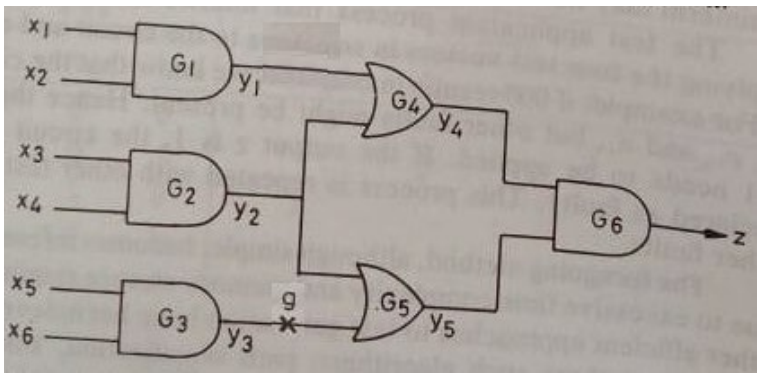
Part B

Answer the Questions. **Total Marks 80M**

11.	**a.**	At the switch level, a transistor can be stuck open or stuck short. These fault models cannot accurately reflect the behaviour of faults in CMOS logic circuits because of multiple transistors used. Illustrate the concept of above stuck faults in 2 input CMOS NAND gate with the help of truth table and explanation?	**10 Marks**	**L2**	**CO1**
	b.	The VLSI development process is a structured, multi-stage methodology transforming a conceptual idea into a physical silicon chip, involving system specifications, logic design, functional verification, physical design (layout), and fabrication. Explain different levels of abstraction in VLSI design verification?	**10 Marks**	**L3**	**CO1**
		Or			
12.	**a.**	The number of failures in 10 power 9 hours is a unit (abbreviated FITS) that is often used in reliability calculations. There is a system with 200 components where each component has a failure rate of 1000 FITS, yield is 60% with fault coverage as 20% and system availability as 99.999%. Calculate the overall failure rate, MTBF, MTTR, repair rate, and defect level, for this system with necessary formulas?	**10 Marks**	**L2**	**CO1**
	b.	Bridging faults are those faults that involve a short between two signal lines in the digital circuit. The logic behaviour of a short defect between signal lines is commonly represented by the	**10 Marks**	**L3**	**CO1**

		bridge fault model. Illustrate the concept of above faults with an example using truth table and explanation?			

13.	**a.**	Scan design in DFT is a technique that replaces standard flip-flops with scan-enabled cells, connecting them into chains to boost controllability and observability. Explain about Clocked Scan Cell design and operation with suitable diagrams and waveforms?	**10 Marks**	**L2**	**CO3**
	b.	What are the SCOAP Combinational Controllability Calculation Rules for 1-Controllability (Primary Input, Output, Branch) of AND, OR, NOT gates. Calculate the SCOAP based Combinational Controllability and Observability measures for the following circuit? 	**10 Marks**	**L3**	**CO2**
		Or			
14.	**a.**	Explain about Partial Scan circuit and test operation of scan architecture with neat sketches?	**10 Marks**	**L2**	**CO3**
	b.	What are the Probability based Controllability Calculation Rules for 1-Controllability (Primary Input, Output, Branch) of AND, OR, NOT gates. Calculate the Probability based Combinational Controllability and Observability measures for the following circuit? 	**10 Marks**	**L3**	**CO2**

15.	**a.**	A) Explain the steps in D algorithm? Generate the test vector for SA0 fault on the line f as shown in figure using table?  B) Draw the D intersection table of above D Algorithm?	**20 Marks**	**L2**	**CO5**
		Or			
16.	**a.**	Find Test vectors for SA-0 Fault at x3 input for the following function using Boolean difference method $((x1 + x2).\overline{x3}) + x3x4$	**10 Marks**	**L2**	**CO5**
	b.	Explain Transistor faults with an example and for the Given circuit if g is having SA1 fault then find the test vector using path sensitization technique? 	**10 Marks**	**L2**	**CO5**

17.	**a.**	Explain BIST with neat sketch? Explain the Logic BIST techniques in detail?	**10 Marks**	**L2**	**CO6**
	b.	Write a detail description about LFSR types and properties with a neat sketch? Generate the test sequence for both types using an example?	**10 Marks**	**L2**	**CO6**
		Or			
18.	**a.**	How test pattern generation is constructed in BIST? Explain in detail with an example	**10 Marks**	**L2**	**CO6**
	b.	Write about serial signature analysis with a neat sketch and generate the signature table for faulty and fault free circuit?	**10 Marks**	**L2**	**CO6**