Roll No.												

PRESIDENCY UNIVERSITY

BENGALURU

End - Term Examinations – May/June 2026

Date: 14 – 05- 2026 **Time:** 01:00pm – 04:00pm

School: SOE	**Program:** B. TECH	
Course Code: ECE3124	**Course Name:** VLSI DESIGN VERIFICATION	
Semester: VI	**Max Marks**: 100	**Weightage**: 50%

CO - Levels	CO1	CO2	CO3	CO4	CO5	CO6
Marks	22	22	48	42	22	24

Instructions:

(i) Read all questions carefully and answer accordingly.

(ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks. **10Q x 2M=20M**

1.	Explain the difference between design and verification in VLSI systems. Give one practical example.	**2 Marks**	**L2**	**CO1**
2.	What is the difference between blocking and non-blocking assignments in Verilog	**2 Marks**	**L2**	**CO3**
3.	Define DUT in RTL simulation and explain its role in testbench environment.	**2 Marks**	**L3**	**CO2**
4.	Define assertion in verification with an example.	**2 Marks**	**L3**	**CO5**
5.	Write a simple Verilog continuous assignment for a 2:1 multiplexer.	**2 Marks**	**L2**	**CO3**
6.	Consider the code: always @(a or b) y = a & b; If input c changes, will output change? Justify based on sensitivity list.	**2 Marks**	**L3**	**CO3**

7.	For a 2-input AND gate, write RTL expression and determine output when A=1, B=0. Explain your answer.	**2 Marks**	**L2**	**CO3**
8.	Define stuck-at fault model with an example.	**2 Marks**	**L1**	**CO6**
9.	A testbench applies inputs but no output is observed from DUT. Identify one possible issue in testbench or DUT connection.	**2 Marks**	**L3**	**CO4**
10.	What is the concept of fault coverage in digital testing?	**2 Marks**	**L2**	**CO6**

Part B

Answer the Questions. **Total Marks 80M**

11.	a.	Explain the complete Digital IC design flow from specification to fabrication. Clearly distinguish between design, verification, and testing.	8 Marks	L2	CO1
	b.	Describe the importance of pre-silicon verification in modern VLSI.	7 Marks	L2	CO1
	c.	Discuss the challenges in verification of large SoC designs.	5 Marks	L2	CO1
		Or			
12.	a.	Explain the different levels of verification (block, subsystem, and SoC) with suitable examples.	8 Marks	L2	CO2
	b.	Describe the types of verification: functional, timing, and testing-oriented.	7 Marks	L2	CO2
	c.	Compare verification tools and their role at different levels.	5 Marks	L2	CO2

13.	**a.**	Apply RTL design concepts to model a 4:1 multiplexer using Verilog (dataflow or behavioral style). Write the complete code and explain its operation.	10Marks	L3	CO3
	b.	Model a D flip-flop with synchronous reset using Verilog (behavioral style).	5 Marks	L3	CO3
	c.	Explain combinational vs sequential always blocks with examples.	5 Marks	L3	CO3
		Or			
14.	a.	Write Verilog code for a 3-bit synchronous up-counter using always block. Simulate the behavior conceptually.	10Marks	L3	CO3
	b.	Differentiate between RTL abstraction and gate-level model.	5 Marks	L2	CO3

	c.	Explain how operators and data types are used in Verilog modeling.	5 Marks	L2	CO3

15.	**a.**	Describe the components of a testbench (DUT, stimulus, monitor) with a block diagram.	8 Marks	L2	CO4
	b.	Explain functional vs timing correctness in verification flow.	6 Marks	L2	CO4
	c.	Develop a simple testbench structure for verifying a combinational circuit in Verilog.	6 Marks	L3	CO4
		Or			
16.	a.	Explain block-level and system-level verification flows with examples.	8 Marks	L2	CO4
	b.	Discuss RTL simulation and debugging concepts.	6 Marks	L2	CO4
	c.	Describe the structure of a testbench with DUT, stimulus, and monitor blocks.	6 Marks	L3	CO4

17.	**a.**	Design a Moore state machine that outputs 1 whenever the binary input sequence “1101” is detected (non-overlapping). Draw the state diagram	6 Marks	L2	CO5
	b.	Write RTL code using always blocks	7 Marks	L3	CO5
	c.	Write testbench to detect “1101” sequence	7 Marks	L3	CO5
		Or			
18.	a.	Explain different types of digital fault models such as stuck-at and bridging faults.	8 Marks	L3	CO6
	b.	Describe the concept of fault simulation and fault coverage.	7 Marks	L3	CO6
	c.	Explain the need for test pattern generation and basics of ATPG.	7 Marks	L3	CO6