Roll No.												

PRESIDENCY UNIVERSITY

BENGALURU

End - Term Examinations – May / June 2026

Date: 20- 05-2026 **Time:**01:00pm – 04:00pm

School: SOE	**Program:** B. Tech	
Course Code: ECE3171	**Course Name:** Microcontroller Applications	
Semester: VI	**Max Marks**: 100	**Weightage**: 50%

CO - Levels	CO1	CO2	CO3	CO4	CO5	CO6
Marks	2	4	28	24	0	42

Instructions:

(i) Read all questions carefully and answer accordingly.

(ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks. **10Q x 2M=20M**

1.	Why is bit-addressable memory preferred in control applications compared to byte-addressable memory?	**2 Marks**	**L2**	**CO1**
2.	How do the mode selection bits in TMOD determine timer operation in 8051?	**2 Marks**	**L3**	**CO3**
3.	How does pipelining efficiency improve in RISC architecture due to fixed instruction length?	**2 Marks**	**L2**	**CO6**

4.	What will be the final value of register A if the CJNE condition is not satisfied in the given program?
	MOV A, #50H
	MOV B, #80H
	ADD A, #30H
	CJNE A, B, NEXT
	SUBB A, #30H
	NEXT: SUBB A, #20H
	END
		2 Marks	**L4**	**CO4**

5.	What happens if the TF0 flag is not cleared after timer overflow?	**2 Marks**	**L2**	**CO3**
6.	What is the effect of executing RR instruction four times on an 8-bit register A?	**2 Marks**	**L4**	**CO4**

7.	Why does 8051 default to register bank 0 after reset?	**2 Marks**	**L3**	**CO2**
8.	In which situations are MOVC and MOVX instructions preferred over MOV?	**2 Marks**	**L2**	**CO2**
9.	The 8051 microcontroller uses an internal machine cycle derived from the crystal oscillator for its operations. How would timer operation change if the machine cycle were different from 12 clock cycles?	**2 Marks**	**L2**	**CO3**
10.	In the 8051-microcontroller assembly programming, control flow is often implemented using flag-based branching instructions. What is the effect of replacing JNB with JB in the given instruction? Again: JNB TF0, Again	**2 Marks**	**L3**	**CO3**

Part B

Answer the Questions. **Total Marks 80M**

11.	**a.**	Explain how instruction set design influences processor performance. Compare RISC and CISC based on execution efficiency and relate it to ARM architecture features.	**10 Marks**	**L3**	**CO6**
		Or			
12.	**a.**	Even though ARM uses more instructions, explain how reduced instruction complexity improves throughput compared to CISC processors	**10 Marks**	**L3**	**CO6**

13.	**a.**	Explain the instruction execution flow in ARM architecture using a block diagram.	**15 Marks**	**L3**	**CO6**
		Or			
14.	**a.**	The ARM architecture is designed for efficient data processing using a streamlined data path. How do components like ALU, register file, and pipeline stages work together to improve ARM processor performance?	**15 Marks**	**L3**	**CO6**

15.	**a.**	Explain the significance of status flags and control bits in CPSR and how they influence processor operation.	**15 Marks**	**L2**	**CO6**
		Or			
16.	**a.**	A processor switches from User mode to IRQ mode during execution. What changes occur in the CPSR during this transition? Why is mode switching important for interrupt handling?	**15 Marks**	**L4**	**CO5**

17.	**a.**	Assembly language is a low-level language that helps to communicate directly with computer hardware. Attempt the following questions: a) Write an ALP such that the addition of two numbers 12H and 13H is performed in subroutine and the sum=25H should be subtracted by 05H in the main program. 5 Marks	**20 Marks**	**L4**	**CO4**

		b) For the given instructions, identify the addressing modes and explain their effect on execution: 5 Marks
		
		MOV R2, #45H
		ADD A, R2
		MOV A, @R1
		ANL A, 30H
		XRL A, #0FH
		
		c) Show the stack and stack pointer for each line of the following program. 5 Marks
		
		MOV R0, #66H
		MOV R3, #7FH
		MOV R7, #5DH
		PUSH 0
		PUSH 3
		PUSH 7
		CLR A
		MOV R3, A
		MOV R7, A
		POP 3
		POP 7
		POP 0
		
		d) Show the status of the CY, AC, and P flags after the addition of 88H and 93H in the following instructions. 5 Marks
		
		MOV A, #88H
		ADD A, #93H			

		Or			
18.	**a.**	a) Write an Assembly Language Program (ALP) to find the smallest number in an array of 5 numbers stored in memory starting from location 30H. Store the result in register A. (5 Marks) b) Explain any five 8051 instructions used for data manipulation with examples. (5 Marks) c) A program performs the following operations: • PUSH 2 • PUSH 4 • PUSH 6 • POP 4 • POP 2 • POP 6 Assuming initial stack pointer = 60H: • Trace the stack contents and SP value after each instruction. (5 Marks)	**20 Marks**	**L3**	**CO2**

		d) Write an ALP to copy 10 bytes of data from one memory location starting at 30H to another location starting at 40H. (5 Marks)			

19.	**a.**	a) Write an ALP to toggle a port pin P1.0 with equal ON and OFF time using software delay. 4Marks b) Write an ALP to generate delay of 0.5 sec using timer-1 and mode-1. 10 Marks c) Explain the TCON register, highlighting the function of each control and flag bit. 6 Marks	**20 Marks**	**L3**	**CO3**
		Or			
20.	**a.**	a) Explain the internal RAM organization of the 8051 microcontrollers. Clearly show the different memory sections. b) Analyze the interrupt handling sequence in 8051, including vector addresses and priority handling, c) Compare polling and interrupt methods for I/O handling with advantages and limitations	**20 Marks**	**L4**	**CO5**