Roll No.												

PRESIDENCY UNIVERSITY

BENGALURU

End - Term Examinations – May / June 2026

Date: 25-05-2026 **Time:** 01:00pm – 04:00pm

School: SOE	**Program:** B. Tech (VLSI)	
Course Code: ECE3177	**Course Name:** Radio Frequency Integrated Circuits & Systems	
Semester: VI	**Max Marks**: 100	**Weightage**: 50%

CO - Levels	**CO1**	**CO2**	**CO3**	**CO4**	**CO5**	**CO6**
Marks	12	12	14	14	24	24

Instructions:

(i) Read all questions carefully and answer accordingly.

(ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks. **10Q x 2M=20M**

1.	What is meant by resonance in the context of a series RLC circuit? State the mathematical condition that must be satisfied for resonance to occur, and briefly state its consequent effect on the impedance characteristics of the circuit.	**2 Marks**	**L1**	**CO1**
2.	A series RLC circuit has R = 100 Ω, L = 0.05 H, and C = 0.6 μF. Calculate the resonant frequency and the Q-factor of the circuit.	**2 Marks**	**L1**	**CO2**
3.	Bring out the fundamental differences between lumped and distributed parameter circuit models. Briefly state the criterion that determines the validity of approximating a transmission line as a lumped parameter system.	**2 Marks**	**L2**	**CO3**
4.	State the unit in which Noise Figure is expressed. Write the Friis formula that governs the overall Noise Figure of a multi-stage cascaded radio receiver system and identify each term in the expression.	**2 Marks**	**L2**	**CO3**

5.	The input signal power and input noise power of a radio receiver are 2 mW and 20 μW respectively. Determine the input Signal-to-Noise Ratio expressed in decibels.	**2 Marks**	**L2**	**CO4**
6.	Briefly explain the significance of the Intermediate Frequency (IF) stage in the architecture of a superheterodyne receiver.	**2 Marks**	**L2**	**CO4**
7.	State the mathematical expression for the efficiency of a Class-B complementary symmetry push-pull amplifier. Under what condition does this efficiency reach its maximum value, and what is that maximum value?	**2 Marks**	**L2**	**CO5**
8.	State the significance of the LC tank circuit employed at the output stage of a Class-C tuned transistor power amplifier.	**2 Marks**	**L3**	**CO5**
9.	Explain the role played by the Voltage Controlled Oscillator (VCO) in the operation of a Phase-Locked Loop (PLL) system.	**2 Marks**	**L3**	**CO6**
10.	What are the principal constraints and challenges that arise in the direct on-chip integration of an antenna within a RFIC design?	**2 Marks**	**L3**	**CO6**

Part B

Answer the Questions. **Total Marks 80M**

11.	**a.**	Concisely describe the operating principle of a class-A power amplifier, supporting your explanation with an appropriate circuit schematic and the corresponding output characteristic waveform.	**10 Marks**	**L1**	**CO1**
	b.	A Class-A power amplifier is designed for an RF transmitter operating at 3.6 GHz. The amplifier uses a single transistor with the following specifications and operating conditions: • Supply voltage: V_{DD} = 10 V • DC bias current: I_{DC} = 100 mA • Load resistance: R_L = 50 Ω • Output power at 1-dB compression point: P_1 dB = 20 dBm • The amplifier delivers a sinusoidal RF output signal with peak voltage swing of 3 V Calculate: (a) The DC power consumed by the amplifier (P_{DC}). (b) The output RF power delivered to the load (P_{out}). (c) The power-added efficiency (PAE) of the amplifier, assuming input power P_{in} = 10 mW. (d) The drain efficiency (η) of the amplifier.	**10 Marks**	**L1**	**CO2**
		Or			
12.	**a.**	With the aid of a suitable circuit schematic and the relevant output characteristic waveforms, concisely describe how a Class-B complementary symmetry push-pull power amplifier operates, clearly identifying the role of each complementary transistor during the positive and negative half-cycles of the input signal.	**10 Marks**	**L1**	**CO1**

	b.	A complementary-symmetry Class-B power amplifier drives a loudspeaker of R_L = 8 Ω from a ±16 V supply. Determine: (a) Maximum AC output power (b) DC input power at maximum output (c) Maximum efficiency (d) Maximum power dissipation per transistor and the condition (Vm) at which it occurs.	**10 Marks**	**L1**	**CO2**

13.	**a.**	Using a circuit diagram and output waveform, briefly explain how a Class-C tuned amplifier works.	**10 Marks**	**L2**	**CO3**
	b.	A Class-C RF power amplifier is to deliver 10 W to a 100 Ω load. Supply voltage VCC = 50 V. Assume ideal transistor (VCE(sat) = 0). Operating frequency f = 5 MHz. The circuit operates at efficiency η = 85%. Find: (a) DC input power P_{dc} (b) Power dissipated in the transistor P_D (c) Peak collector current $I_{c(max)}$ required (d) Peak collector-emitter voltage $V_{CE(peak)}$ (e) Inductance L of the tank circuit (for C = 50 pF).	**10 Marks**	**L2**	**CO4**
		Or			
14.	**a.**	Explain the working principle of a Phase-Locked Loop (PLL) used in RF receivers. With the help of a neat block diagram, describe the function of each building block of a PLL.	**10 Marks**	**L2**	**CO3**
	b.	What is a Voltage-Controlled Oscillator (VCO)? Explain its role in a PLL-based frequency synthesizer used in RF receivers.	**10 Marks**	**L2**	**CO4**

15.	With the help of a neat circuit diagram, explain the working principle of a Hartley Oscillator. Describe the role of each component in the circuit, explain how sustained oscillations are produced, and discuss the advantages, disadvantages, and practical applications of the Hartley Oscillator in communication systems.	**20 Marks**	**L3**	**CO5**
	Or			
16.	With the aid of a clearly labeled circuit diagram, explain the construction and working of a Colpitts Oscillator. Discuss how the capacitive voltage divider network provides the necessary feedback for sustained oscillations. Also, compare the Colpitts Oscillator with the Hartley Oscillator in terms of circuit structure, feedback mechanism, stability, and frequency range of operation.	**20 Marks**	**L3**	**CO5**

17.	With the help of a neat block diagram, explain the architecture of a modern RF transceiver. Describe the key functional blocks involved in transmission and reception. Discuss how transceiver design considerations differ for Wi-Fi, 5G, and IoT applications in terms of frequency band, power consumption, data rate, and range.	**20 Marks**	**L3**	**CO6**
	Or			

18.	With the help of a neat diagram, explain how antennas are integrated with Radio Frequency Integrated Circuits (RFICs). Describe the challenges involved in antenna-RFIC integration and discuss the impact of antenna parameters such as impedance matching, radiation efficiency, and bandwidth on the overall performance of the RFIC-based wireless system.	**20 Marks**	**L3**	**CO6**