Roll No.												

PRESIDENCY UNIVERSITY

BENGALURU

End - Term Examinations – MAY /JUNE 2026

Date: 22 / 05/ 2026 **Time:** 01:00pm – 04:00pm

School: SOE	**Program:** B. TECH -VLSI	
Course Code :: ECE3179	**Course Name:** Physical Design and Automation	
Semester: VI	**Max Marks:**100	**Weightage:** 50%

CO - Levels	CO1	CO2	CO3	CO4	CO5
Marks	14	14	24	24	24

Instructions:

(i) Read all questions carefully and answer accordingly.

(ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks. 10Q x 2M=20M

1	Define the concept of structural design in VLSI and its role in representing the arrangement and interconnection of logic gates in digital circuits.	**2 Marks**	**L1**	**CO1**
2	Define any two verification methods used in physical design and their significance in ensuring that the layout meets functional correctness and design rules.	**2 Marks**	**L1**	**CO1**
3	Define the concept of partitioning in VLSI design and its purpose in dividing large circuits into smaller blocks for easier placement and routing.	**2 Marks**	**L1**	**CO2**

4	Define the concept of symbolic layout in VLSI and its importance in abstracting the physical design to assist in floorplanning and placement.	**2 Marks**	**L1**	**CO2**
5	Define the concept of a routing channel and its role in connecting circuit components, assigning tracks, and supporting efficient interconnections.	**2 Marks**	**L1**	**CO4**
6.	Define the main objectives of floorplanning in VLSI and its impact on chip area, interconnect length, routing efficiency, and overall circuit performance.	**2 Marks**	**L1**	**CO3**
7.	Define the aspect ratio in floorplanning and its significance in calculating dimensions and ensuring efficient placement of blocks on a chip.	**2 Marks**	**L1**	**CO3**
8.	Define the concept of local routing in VLSI design and its function in connecting pins within a small region while resolving conflicts and maintaining spacing and timing.	**2 Marks**	**L1**	**CO4**
9.	Define Reduced Ordered Binary Decision Diagram (ROBDD) and its structure, purpose in logic representation, and utility in optimizing Boolean functions.	**2 Marks**	**L1**	**CO5**
10.	Define high-level transformations in VLSI design and state their purpose.	**2 Marks**	**L1**	**CO5**

Part B

Answer the Questions. **Total Marks 80M**

11.	VLSI design is carried out through a sequence of well-defined stages supported by EDA tools. With the help of a neat and well-labelled flow diagram, describe the complete VLSI design flow using EDA tools, starting from system specification and architectural design to physical design and final verification. Describe the objectives, inputs, and outputs of each design stage.	**10 Marks**	**L2**	**CO1**
	Or			
12.	Verification is a critical activity in ensuring the correctness and reliability of VLSI designs. Describe the various verification methods used in VLSI design automation, including functional, timing, and physical verification techniques. describe the role of each verification method at different abstraction levels.	**10 Marks**	**L2**	**CO1**

13.	Layout compaction plays a crucial role in optimizing VLSI physical design. With reference to this statement, analyse the necessity of layout compaction in modern integrated circuit design.	**10 Marks**	**L3**	**CO2**
	Or			
14.	Partitioning is a fundamental step in handling large VLSI designs. In this context, analyse the working principle of the Kernighan–Lin (KL) partitioning algorithm, including initial partition formation, gain computation, node exchange strategy, and convergence behaviour. Apply the effectiveness of the algorithm in minimizing cut size, and critically assess its advantages, limitations, and computational complexity when applied to large-scale circuits.	**10 Marks**	**L3**	**CO2**
15.	In VLSI chip design, connecting all circuit components efficiently is critical to achieving high performance, minimal delay, and optimal area utilization. Routing plays a vital role in this process and is generally divided into global routing, which plans approximate paths across the chip, and local routing, which finalizes detailed connections within smaller regions.Apply the roles of global routing and local routing in VLSI physical design.	**10 Marks**	**L3**	**CO3**
	Or			
16.	Floor planning is the process of arranging functional blocks on a chip to optimize area, interconnect length, and routing. Apply concepts of floor planning in VLSI physical design to determine an effective floor plan for a given chip specification, including the identification of objectives, execution of key steps such as chip sizing, aspect ratio selection, macro placement, and power planning, addressing design challenges, and demonstrating how the resulting floor plan improves area utilization, routing efficiency, and overall chip performance. ion.	**10 Marks**	**L3**	**CO3**
17.	Assignment and scheduling in high-level synthesis involve allocating operations to functional units and assigning clock cycles to each operation to meet timing, area, and resource constraints while optimizing performance.Describe assignment and scheduling in high-level synthesis, including their objectives, differences, constraints, and roles in optimizing hardware resources, execution time, and overall system performance.	**10 Marks**	**L2**	**CO5**
	Or			
18.	The hardware model in high-level synthesis represents a digital system using functional units, registers, and interconnections to capture its behavior at the algorithmic or RTL level, enabling automated scheduling, allocation, and binding for efficient hardware implementation.Describe the hardware model for high-level synthesis, including the transformation of behavioural descriptions into structural representations, the roles of functional units, registers, multiplexers, and interconnection networks, and the processes of scheduling, allocation, and binding in achieving efficient hardware implementation.	**10 Marks**	**L2**	**CO5**

19.	Abstraction levels in VLSI are hierarchical design stages—from system-level (functional specification), algorithmic/behavioral level, register-transfer level (RTL), gate level, and transistor/circuit level—that allow designers to manage complexity, optimize performance, and map high-level designs to physical silicon efficiently.Analyse the three major abstraction levels in VLSI design, namely structural design, logic design, and transistor-level design. For each level, describe the design objectives, representation techniques, constraints, and typical applications.	**10 Marks**	**L4**	**CO4**
	Or			
20.	Two-level logic synthesis implements Boolean functions in sum-of-products (SOP) or product-of-sums (POS) form, and optimization techniques like Boolean factoring, common subexpression sharing, and redundancy removal reduce gate count, minimize delay, and improve hardware efficiency in digital system design.Analyse the significance of two-level logic synthesis in digital system design optimization techniques, such as Boolean factoring and redundancy removal, affect circuit performance, power consumption, and hardware efficiency in VLSI implementations.	**10 Marks**	**L4**	**CO4**

21.	Constraint graph–based compaction algorithms model horizontal and vertical spacing constraints between circuit blocks as a graph and then compute optimal positions to minimize area while satisfying all design rules in VLSI layouts.Apply constraint graph–based compaction algorithms to optimize a given VLSI layout, including the formulation of constraints, construction of horizontal and vertical constraint graphs, identification of critical paths, and demonstration of how compaction reduces layout area while satisfying design rules and spacing constraints.	**10 Marks**	**L3**	**CO3**
	Or			
22.	The FM algorithm is designed to partition a circuit (or graph) into two balanced parts while minimizing the cutsize — i.e., the number of connections between the two partitions. It's commonly used in standard cell placement, floorplanning, and netlist partitioning.Use Fiduccia–Mattheyses (FM) partitioning algorithm, focusing on data structures used, gain computation strategy, pass-based optimization process, and stopping conditions. Show how the FM algorithm improves partition quality.	**10 Marks**	**L3**	**CO3**

23.	Channel routing connects pins in a predefined channel between rows of components using track assignment and left-edge/dogleg methods, whereas area routing connects nets across the entire chip area using grid- or graph-based algorithms while handling obstacles, congestion, and multiple layers.Describe channel routing and area routing techniques in VLSI physical design, including their principles, routing models, constraints, algorithms, advantages, limitations, and their impact on routing efficiency, area utilization, and overall chip performance.	**10 Marks**	**L2**	**CO4**

	Or			
24.	Local routing connects pins within a small region to resolve short-range connections, while area routing handles complex, chip-wide net connections across multiple blocks and layers.Describe local routing and area routing techniques used in VLSI design, including their routing methodologies, design considerations, constraints, advantages, limitations, and their impact on congestion, wirelength, and overall chip performance.	**10 Marks**	**L2**	**CO4**

25.	Routing algorithms are computational methods used to find these paths efficiently while satisfying design rules, minimizing delay, and optimizing area usage.Differentiate routing algorithms used in VLSI physical design, including Lee's algorithm, Negotiated algorithm, A* algorithm, Line Search algorithm, and Steiner Tree algorithm, in terms of their principles, path optimality, computational complexity, memory requirements, advantages, disadvantages, and suitability for different routing scenarios.	**10 Marks**	**L2**	**CO5**
	Or			
26.	Combinational logic synthesis is the process of designing and optimizing a digital circuit that produces outputs solely based on the current inputs (without memory or feedback). The goal is to transform a high-level Boolean specification into an optimized network of logic gates that meets area, speed, and power constraints.Describe the principles of combinational logic synthesis, including Boolean function representation, minimization techniques, and optimization goals, the concept of Reduced Ordered Binary Decision Diagram (ROBDD) including its properties, construction procedure, implementation methods, and manipulation operations, and its role and significance in two-level logic synthesis for achieving efficient, optimized, and reduced-complexity digital circuit design.	**10 Marks**	**L2**	**CO5**