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Bengaluru

Mid Term Examinations - October 2026

Date: 05/10/2026 **Time:** 09:30 AM - 11:00 AM

Course Code: CSS2257 **Course Name:** Computer Organization and Architecture

Semester: Fifth Semester **Max. Marks:** 50 **Weightage:** 50%

CO - Levels	CO1	CO2
Marks	92	88

PART A: Answer Following Questions. 10 M

Q.N.	Questions	M	CO	BT
1	Explain briefly why the Program Counter (PC) is incremented during the fetch cycle.	2	CO1	BT2
2	List the five functional units of a digital computer.	2	CO1	BT1
3	Compare between a Single Bus and a Multiple Bus organization.	2	CO1	BT2
4	Define Cache Memory and state its purposes.	2	CO2	BT1
5	Define stack and Stack Pointer (SP).	2	CO2	BT1

PART B : Answer Any 1 Following Questions. 10 M

Q.N.	Questions	M	CO	BT
6	a)Explain the basic performance equation of a computer and identify the factors affecting CPU execution time with example. (5m) b)Solve a Program, which has 100 machine instructions in a straight line code and 100 instructions in a loop which gets executed for 49 times. The average number of basic steps needed to execute one machine instruction is 2 cycles and the processor is controlled by a clock of 2GHz. Find the time required for the program execution. (5m)	10	CO1	BT3
7	a) Explain the concept of the Program Counter (PC), Instruction Register (IR) and Memory Address Register (MAR) in the context of the instruction cycle, with the help of a diagram. (5m) b)A program contains 1000 instructions. Out of that 25% instructions requires 4 clock cycles, 40% instructions requires 5 clock cycles and remaining requires 3 clock cycles for execution. Find the total time required to execute the program running in a 1 GHz machine. (5m)	10	CO1	BT3

PART C: Answer Any 1 Following Questions. 10 M

Q.N.	Questions	M	CO	BT
8	a)List and briefly explain the four basic instruction formats — Zero-address, One-address, Two-address and Three-address — with one example instruction for each.(5m) b) Construct the assembly language instraction for the equation, E=(A+B) X (C+D) using all instruction formats. (5m)	10	CO1	BT3

9	Represent –47 and +25 in 8-bit two's complement form and perform the coresponding operation a)(−47) − (+25) using 2's complement arithmetic. b)(-100) + (-50) using 2"s complement arithmetic. Verify the result and comment on overflow, if any.	10	CO1	BT3

PART D: Answer Any 1 Following Questions. 10 M				
Q.N.	**Questions**	**M**	**CO**	**BT**
10	Explain any five addressing modes used in instruction set architecture with suitable examples for each.	10	CO2	BT2
11	Explain the internal organization of 16 x 4 memory chip with a neat diagram.	10	CO2	BT2

PART E: Answer Any 1 Following Questions. 10 M				
Q.N.	**Questions**	**M**	**CO**	**BT**
12	a) Describe the concepts of 'Cache Hit' and 'Cache Miss' and describe how the hit ratio affects the average memory access time. Write the formula used to calculate the average memory access time. (5 Marks) b)Explain the fundamental operational differences between Direct Mapping, Associative Mapping (Fully Associative), and Set-Associative Mapping techniques in cache memory(5m).	10	CO2	BT2
13	a) Explain the PUSH and POP operations on a stack with a neat diagram, showing the effect on the Stack Pointer. (5m) b)Explain the steps involved in calculating the sum of 5 array elements using a subroutine with register parameter passing in assembly language. (5m)	10	CO2	BT2