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Bengaluru

Mid Term Examinations - October 2026

Date: 06/10/2026 **Time:** 11:45 AM - 01:15 PM

Course Code: ECE2514 **Course Name:** Design for Testability

Semester: Fifth Semester **Max. Marks:** 50 **Weightage:** 50%

CO - Levels	CO1	CO2	CO3
Marks	46	24	20

PART A: Answer Following Questions. 10 M

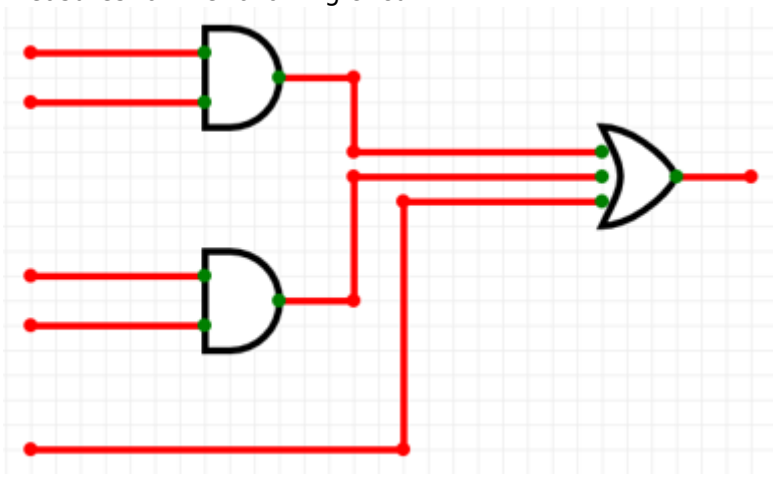
Q.N.	Questions	M	CO	BT
1	Testing typically consists of applying a set of test stimuli to the inputs of the circuit under test (CUT) while analyzing the output responses, Circuits that produce the correct output responses for all input stimuli pass the test.What are the two undesirable situations that occur during testing of IC?	2	CO1	BT1
2	Electronic testing includes Integrated circuit testing, printed circuit board (PCB) testing, and system testing at the various manufacturing stages and, in some cases, during system operation. Testing is used not only to find the fault-free devices, PCBs, and systems but also to improve production yield at the various stages of manufacturing by analysing the cause of defects when faults are encountered. Expand CUT, ATE?	2	CO1	BT1
3	Suppose the system is in normal operation at t = 0, it fails at t1, and the normal system operation is recovered at t2 by some software modification, reset, or hardware replacement and if repair rate is 10. Then what is the value of MTTR?	2	CO1	BT1
4	Test engineers usually have to construct test vectors after the design is completed. This invariably requires a substantial amount of time and effort that could be avoided if testing is considered early in the design flow to make the design more testable. What are the different categories in DFT techniques?	2	CO2	BT1
5	Testability analysis refers to the process of assessing the testability of a logic circuit by calculating a set of numerical measures for each signal in the circuit.What is the full form of SCOAP and what are the calculation parameters ?	2	CO2	BT1

PART B : Answer Any 1 Following Questions. 10 M

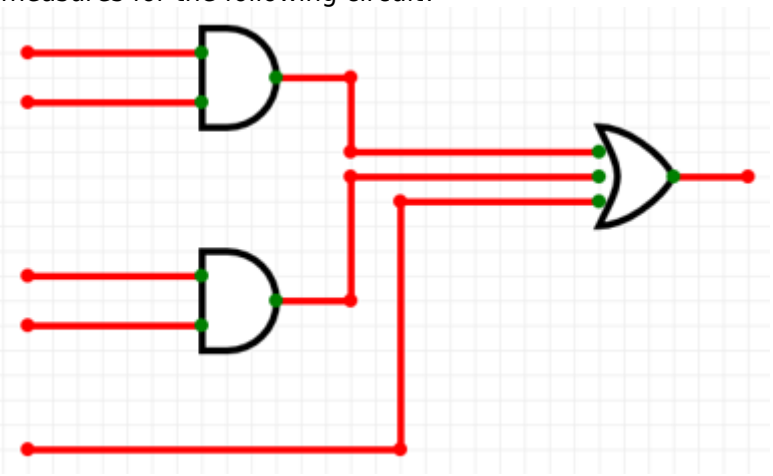
Q.N.	Questions	M	CO	BT
6	At the switch level, a transistor can be stuck open or stuck short. These fault models cannot accurately reflect the behaviour of faults in CMOS logic circuits because of multiple transistors used. Illustrate the concept of above stuck faults in 2 input CMOS NOR gate with the help of truth table and explanation?	10	CO1	BT2
7	It can be seen that some form of testing is involved at each stage of the VLSI testing process. Based on a customer or project need, a VLSI device requirement is determined and formulated as a design specification. Explain VLSI Development process with neat sketch?	10	CO1	BT2

PART C: Answer Any 1 Following Questions. 10 M

Q.N.	Questions	M	CO	BT
8	The number of failures in 10 power 9 hours is a unit (abbreviated FITS) that is often used in reliability calculations. There is a system with 100 components where each component has a failure rate of 1000 FITS, yield is 50% with fault coverage as 10% and system availability as 99.999%. Calculate the overall failure rate, MTBF, MTTR, repair rate, and defect level, for this system with necessary formulas?	10	CO1	BT2
9	A short between two elements is commonly referred to as a bridging fault. These elements can be transistor terminals or connections between transistors and gates. The case of an element being shorted to power (VDD) or ground (VSS) is equivalent to the stuck-at fault model; however, when two signal wires are shorted together, bridging fault models are required. Illustrate the concept of above faults with an example using truth table and explanation?	10	CO1	BT2

PART D: Answer Any 1 Following Questions. 10 M				
Q.N.	**Questions**	**M**	**CO**	**BT**
10	Scan design, the most widely used structured DFT methodology, attempts to improve testability of a circuit by improving the controllability and observability of storage elements in a sequential design. Typically, this is accomplished by converting the sequential design into a scan design with different modes of operations. Explain about Edge triggered Muxed D Scan Cell design and operation with suitable diagrams and waveforms?	10	CO3	BT2
11	What are the SCOAP Combinational Controllability Calculation Rules for 0-Controllability (Primary Input, Output, Branch) of AND, OR, NOT gates. Calculate the SCOAP based Combinational Controllability and Observability measures for the following circuit? 	10	CO2	BT2

PART E: Answer Any 1 Following Questions. 10 M				
Q.N.	**Questions**	**M**	**CO**	**BT**
12	In Scan architecture, all storage elements are replaced with scan cells, which are then configured as one or more shift registers (also called scan chains). Explain about Full Scan circuit and test operation of scan architecture with neat sketches?	10	CO3	BT2

13	What are the Probability based Controllability Calculation Rules for 0-Controllability (Primary Input, Output, Branch) of AND, OR, NOT gates. Calculate the Probability based Combinational Controllability and Observability measures for the following circuit? 	10	CO2	BT2