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Bengaluru

Mid Term Examinations - October 2026

Date: 07/10/2026 **Time:** 02:00 PM - 03:30 PM

Course Code: ECE2522 **Course Name:** CMOS VLSI Design

Semester: Fifth Semester **Max. Marks:** 50 **Weightage:** 50%

CO - Levels	CO1	CO2	CO3
Marks	26	24	40

PART A: Answer Following Questions. 10 M

Q.N.	Questions	M	CO	BT
1	Illustrate the body effect of the MOSFET transistors.	2	CO1	BT1
2	Differentiate short and long channel devices.	2	CO1	BT1
3	List out the various terminal and virtual capacitances of a MOSFET.	2	CO2	BT1
4	Illustrate the channel-length modulation of the MOSFET transistors.	2	CO1	BT1
5	List the advantages and disadvantages of saturation and linear load nmos inverters.	2	CO2	BT1

PART B : Answer Any 1 Following Questions. 10 M

Q.N.	Questions	M	CO	BT
6	The drain current (ID) equation for a MOSFET depends on its operating region, with distinct formulas for the linear (or triode) and saturation regions. Derive the drain current equation of MOSFET both linear and saturation regions.	10	CO1	BT2
7	“Channel length" refers to the effective length of the conductive path in a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor), which is the distance between the source and drain electrodes. Describe channel length modulation with a neat diagram and derive the expression for the same.	10	CO1	BT2

PART C: Answer Any 1 Following Questions. 10 M

Q.N.	Questions	M	CO	BT
8	The main advantage of using a MOSFET as a load device is that the silicon area occupied by the transistor is smaller than the area occupied by the resistive load. Explain the depletion load nmos Inverter with a neat diagram.	10	CO2	BT2
9	CMOS inverter is a basic digital logic circuit that uses NMOS and PMOS to perform a logical inversion. Discuss CMOS inverter and draw the VTC of the CMOS inverter with suitable mathematical equations.	10	CO2	BT3

PART D: Answer Any 1 Following Questions. 10 M

Q.N.	Questions	M	CO	BT
10	The fabrication on a silicon wafer is done with the help of layout diagrams, and all the layers in layout are represented by its length and widths. Draw the stick and layout diagrams of two input NAND Gate using Euler’s method.	10	CO3	BT2

11	The fabrication on a silicon wafer is done with the help of layout diagrams, and all the layers in the layout are represented by its length and widths. Draw the stick and layout diagrams of two input NOR gate using Euler's method.	10	CO3	BT2

PART E: Answer Any 1 Following Questions. 10 M				
Q.N.	**Questions**	**M**	**CO**	**BT**
12	Current Mirrors are particularly useful in the integrated circuits, for biasing the amplifiers. Discuss the MOSFET current mirror circuit.	10	CO3	BT2
13	MOSFETs are electronic devices used to switch or amplify voltages in circuits. Discuss MOS as a switch, as a diode, and as a resistor.	10	CO3	BT2