Roll No: | | | | | | | | | | | |

PRESIDENCY UNIVERSITY

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GAIN MORE KNOWLEDGE
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Mid Term Examinations - October 2026

Date: 06/10/2026 **Time:** 02:00 PM - 03:30 PM

Course Code: ECE3047 **Course Name:** CAD for VLSI

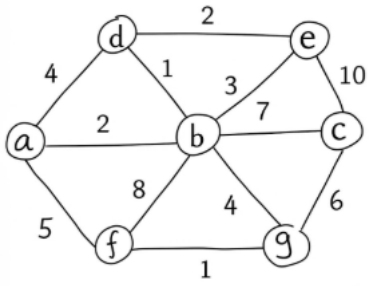
Semester: Seventh Semester **Max. Marks:** 50 **Weightage:** 50%

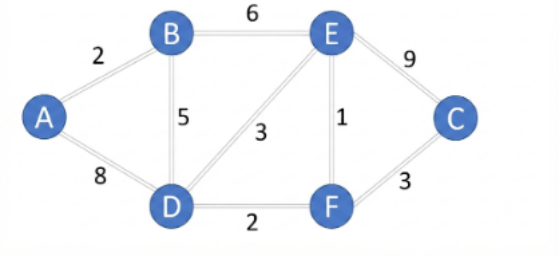
CO - Levels	CO1	CO2
Marks	44	46

PART A: Answer Following Questions. 10 M

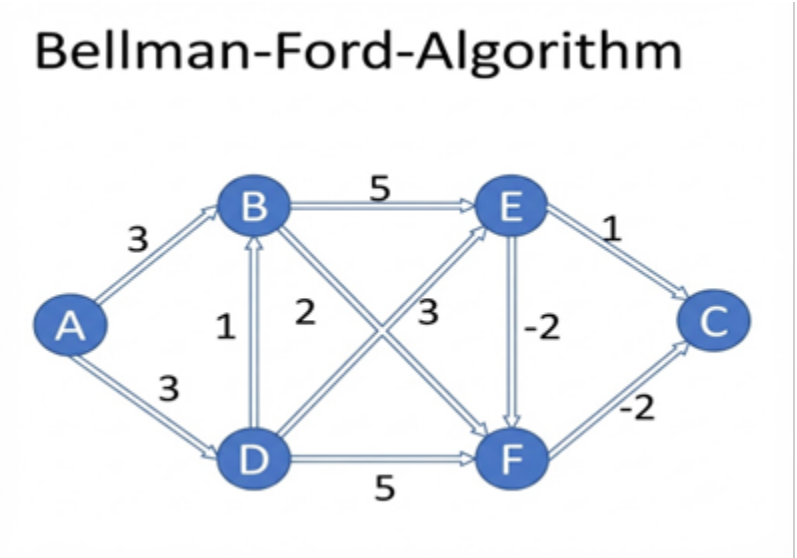
Q.N.	Questions	M	CO	BT
1	Define an Adjacency Matrix representation of a graph.	2	CO1	BT1
2	Define Gate Array Design.	2	CO1	BT1
3	Define Polynomial-Time Reduction.	2	CO2	BT1
4	Define a Rectilinear Steiner Tree (RST) in VLSI routing.	2	CO2	BT1
5	Define Symbolic Layout in VLSI design.	2	CO2	BT1

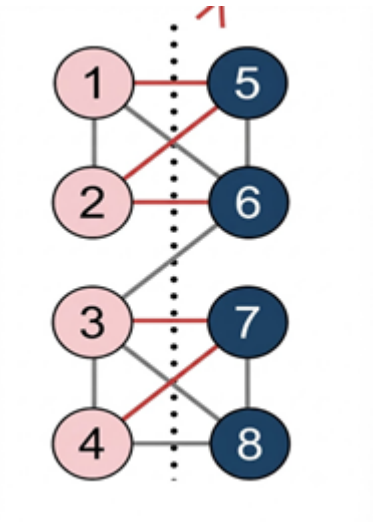
PART B : Answer Any 1 Following Questions. 10 M

Q.N.	Questions	M	CO	BT
6	 Given a connected, weighted, undirected graph with vertices A, B, C, D, E, F G and the following weighted edges: shown in the figure, apply Prim's algorithm starting from vertex A to determine the Minimum Spanning Tree (MST) of the graph and calculate its total minimum cost.	10	CO1	BT3

7	Dijkstra's Shortest Path Algorithm  Given a weighted, connected graph with vertices , apply Dijkstra's algorithm by taking vertex A as the source vertex to determine the shortest path from A to every other vertex and calculate the corresponding shortest-path distances.	10	CO1	BT3

PART C: Answer Any 1 Following Questions. 10 M				
Q.N.	**Questions**	**M**	**CO**	**BT**
8	In the development of an integrated circuit, a systematic sequence of design and implementation stages is required to convert the initial system requirements into a manufacturable chip. Explain the concept and purpose of the VLSI Design Flow, describe the sequence and role of the major stages, from system specification, architectural design, RTL design, functional verification, logic synthesis, physical design, and physical verification to final chip fabrication, with the complete flow using a neat block diagram.	10	CO1	BT2
9	In VLSI design, different levels of abstraction are used to represent and develop a digital system systematically. Explain the Gajski–Kuhn (Y-Chart) model and describe the Behavioral, Structural, and Physical design domains, including their purpose, relationship, and suitable examples for each domain, with a neat representation of the Y-Chart.	10	CO1	BT2

PART D: Answer Any 1 Following Questions. 10 M				
Q.N.	**Questions**	**M**	**CO**	**BT**
10	Bellman-Ford-Algorithm  In a weighted directed graph, where some edges may have negative weights, apply the Bellman–Ford algorithm by taking vertex A as the source, to determine the shortest path from A to C, showing the distance updates after each iteration and verifying whether the graph contains any negative-weight cycle.	10	CO2	BT3

11	 In VLSI physical design, where reducing the total interconnection length is essential for improving chip performance, apply the Kernighan–Lin (KL) algorithm to partition the given set of cells into two equal-sized groups, showing the sequence of cell exchanges, calculating the gain for each possible exchange, and identifying the final partition with minimum interconnection cost.	10	CO2	BT3

PART E: Answer Any 1 Following Questions. 10 M				
Q.N.	**Questions**	**M**	**CO**	**BT**
12	In algorithm analysis, complexity is used to describe the resources required by an algorithm as the input size increases. Explain the concept of complexity and algorithm complexity, including time complexity and space complexity, with suitable examples.	10	CO2	BT2
13	Computational problems can be classified based on the time required to solve or verify their solutions as the input size increases. Explain the role of algorithm complexity in classifying computational problems into P, NP, and NP-Complete classes with suitable examples.	10	CO2	BT2