Roll No: | | | | | | | | | | | |

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

PRESIDENCY UNIVERSITY

Presidency University Act, 2013 of the Karnataka Act No. 41 of 2013 | Established under Section 2(f) of UGC Act, 1956
Approved by AICTE, New Delhi | Approved By BCI
Bengaluru

Mid Term Examinations - October 2026

Date: 06/10/2026 **Time:** 02:00 PM - 03:30 PM

Course Code: ECE3192 **Course Name:** Digital Design using Hardware Description Language

Semester: Seventh Semester **Max. Marks:** 50 **Weightage:** 50%

CO - Levels	CO1	CO2
Marks	44	46

PART A: Answer Following Questions. 10 M

Q.N.	Questions	M	CO	BT
1	For the given statement, how many memory locations are there in R1 and in each memory location how many bits are stored? reg [15: 0] R1[511 :0]?	2	CO1	BT1
2	How many ports are supported by verilog and what are they?	2	CO1	BT1
3	What are the different delays associated with the given statement bufif1 #(1:2:3, 2:4:6, 3:6:9) g3 (a0, b0, c0);	2	CO2	BT1
4	Write the functional description for bufif1?	2	CO2	BT1
5	If a= 5'b11011; d=a>>1, then value of d in binary is?	2	CO2	BT1

PART B : Answer Any 1 Following Questions. 10 M

Q.N.	Questions	M	CO	BT
6	Discuss the FPGA and ASIC design flows and compare them in terms of flexibility, performance using suitable flow diagrams?	10	CO1	BT2
7	Explain different levels of Design Description with examples? Write a Verilog Module and test bench for half subtractor in structural style?	10	CO1	BT2

PART C: Answer Any 1 Following Questions. 10 M

Q.N.	Questions	M	CO	BT
8	What are different Data Types in Verilog? Write a Verilog module and test bench for 3-8 decoder using basic gates in structural style?	10	CO1	BT2
9	Explain the Following terms: a) Concurrency b) Simulation c) Synthesis d) PLI	10	CO1	BT2

PART D: Answer Any 1 Following Questions. 10 M

Q.N.	Questions	M	CO	BT
10	Write a verilog module in structural style and testbench for SR Latch using nor gates with neat sketch?	10	CO2	BT2
11	Write a verilog module in structural style and testbench for Full adder using half adder and single OR primitive with neat sketch?	10	CO2	BT2

PART E: Answer Any 1 Following Questions. 10 M

PTO (Please Turn Over)

Q.N.	Questions	M	CO	BT
12	Explain ternary operator (conditional operator) syntax? Write a Verilog module and test bench for 2X1 Mux using ternary operator?	10	CO2	BT2
13	Find the value of the following expressions if the two unsigned variables are A=4'b1010 B=4'b0101 i) {A,B} ii) (A & B) iii) | B iv) (A ^ B) v) ~A	10	CO2	BT2