Roll No: | | | | | | | | | | | |

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

PRESIDENCY UNIVERSITY

Presidency University Act, 2013 of the Karnataka Act No. 41 of 2013 | Established under Section 2(f) of UGC Act, 1956
Approved by AICTE, New Delhi | Approved By BCI
Bengaluru

Mid Term Examinations - October 2026

Date: 05/10/2026 **Time:** 02:00 PM - 03:30 PM

Course Code: ECE3413 **Course Name:** Low Power VLSI Design

Semester: Fifth Semester **Max. Marks:** 50 **Weightage:** 50%

CO - Levels	CO1	CO2
Marks	48	42

PART A: Answer Following Questions. 10 M

Q.N.	Questions	M	CO	BT
1	Power consumption is a critical consideration in modern CMOS VLSI circuits because it affects battery life, thermal management, reliability, and overall system performance. Name the different static and dynamic power dissipation sources in CMOS VLSI circuits.	2	CO1	BT1
2	In CMOS VLSI design, the power dissipation and propagation delay of an inverter are important performance parameters that determine the energy efficiency and speed of a digital circuit. Draw the graphs of inverter power-delay characteristics and power dissipation, and explain the variation of power and delay with the relevant operating parameters.	2	CO1	BT2
3	Dynamic power dissipation is an important consideration in CMOS VLSI circuits because the charging and discharging of load capacitances during logic transitions contributes significantly to total power consumption. A CMOS circuit operates at VDD=1.2V, with a load capacitance of 20pF and switching frequency of 100MHz. If the switching activity factor is 0.5, calculate the dynamic power dissipation.	2	CO1	BT3
4	SPICE is widely used to model and analyze electronic circuits under different operating conditions and helps designers evaluate parameters such as voltage, current, timing, and power consumption. Define SPICE. Mention any two types of analysis performed using a SPICE simulator.	2	CO2	BT1
5	Process, device, and manufacturing variations can cause significant changes in the performance of modern VLSI circuits.Explain Monte Carlo simulation. Mention any two circuit parameters that can be analyzed using Monte Carlo simulation.	2	CO1	BT1

PART B : Answer Any 1 Following Questions. 10 M

Q.N.	Questions	M	CO	BT
6	In modern CMOS VLSI circuits, dynamic power dissipation is a major component of total power consumption and becomes increasingly important as the operating frequency and transistor density increase. Derive the expression for dynamic power dissipation in CMOS circuits.	10	CO1	BT3
7	In CMOS VLSI design, proper sizing of PMOS and NMOS transistors is essential to achieve the desired propagation delay and balanced circuit performance. Determine the dimension of MOSFET for the boolean expression ***(A.B+E(C+D))'*** for the same propagation delay. Given the inverter with PMOS dimensions W/L = 3/1 and NMOS dimensions W/L = 2/1.	10	CO1	BT4

PTO (Please Turn Over)

PART C: Answer Any 1 Following Questions. 10 M				
Q.N.	**Questions**	**M**	**CO**	**BT**
8	Determine the dimension of MOSFET for the boolean expression ***(A.(B+CD))'*** for the same propagation delay. Given the inverter with PMOS dimensions W/L = 3/1 and NMOS dimensions W/L = 2/1.	10	CO1	BT4
9	CMOS technology continues to scale toward smaller device dimensions, leakage currents become increasingly significant and contribute substantially to the overall power consumption of VLSI circuits, particularly during standby operation. Explain the different components of static (leakage) power dissipation in a MOSFET with relevant diagrams.	10	CO1	BT3

PART D: Answer Any 1 Following Questions. 10 M				
Q.N.	**Questions**	**M**	**CO**	**BT**
10	Process and device variations can significantly affect the power and performance of modern VLSI circuits. Explain the principle and methodology of Monte Carlo simulation for VLSI circuits. Discuss the role of statistical variations in transistor parameters, capacitance, threshold voltage, power consumption, and propagation delay, and explain how Monte Carlo analysis is used to assess circuit robustness and yield.	10	CO2	BT4
11	Power analysis can be performed at different levels of abstraction depending on the stage of VLSI design. Explain the hierarchical approach to power analysis at the architecture, RTL, gate, and transistor levels. Discuss the advantages, limitations, accuracy, and applications of power estimation at each level.	10	CO2	BT3

PART E: Answer Any 1 Following Questions. 10 M				
Q.N.	**Questions**	**M**	**CO**	**BT**
12	Accurate capacitance estimation is essential for reliable power analysis of digital VLSI circuits. Explain the methodology of gate-level capacitance estimation. Discuss the contributions of input capacitance, fan-out capacitance, interconnect capacitance, and parasitic capacitance to the total effective capacitance of a logic gate.	10	CO2	BT4
13	Gate-level simulation is an important stage between logic synthesis and physical implementation of a digital VLSI circuit. Explain the concept of gate-level logic simulation and discuss its importance in functional verification, timing analysis, switching-activity estimation, and power analysis.	10	CO2	BT4