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PRESIDENCY UNIVERSITY

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Bengaluru

Mid Term Examinations - October 2026

Date: 05/10/2026 **Time:** 02:00 PM - 03:30 PM

Course Code: ECE3415 **Course Name:** Design for Testability

Semester: Fifth Semester **Max. Marks:** 50 **Weightage:** 50%

CO - Levels	CO1	CO2
Marks	46	44

PART A: Answer Following Questions. 10 M

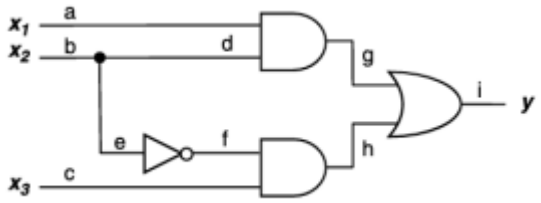
Q.N.	Questions	M	CO	BT
1	Explain the significance of VLSI testing in ensuring the quality and reliability of fabricated ICs.	2	CO1	BT2
2	Define the following terms:i) Defect Level ii) Fault Coverage	2	CO1	BT2
3	Explain the different levels of abstraction used in VLSI design and testing.	2	CO1	BT2
4	State the SCOAP rules for calculating combinational controllability of a two-input AND gate and OR gate.	2	CO2	BT2
5	Explain the importance of Controllability and Observability in testability analysis.	2	CO2	BT2

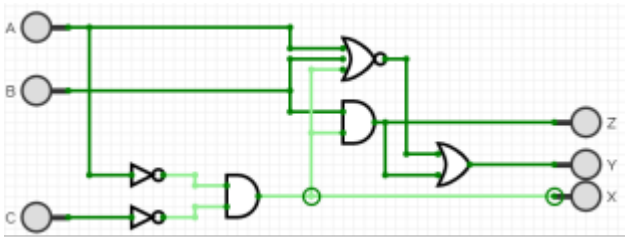
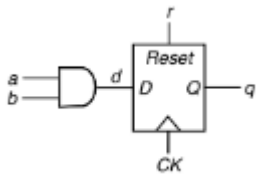
PART B : Answer Any 1 Following Questions. 10 M

Q.N.	Questions	M	CO	BT
6	a)Explain the major stages involved in the VLSI testing life cycle, starting from IC fabrication to final testing.b) Explain the following manufacturing test parameters with suitable examples: i) Yield ii) Yield Loss iii) Reject Rate iv) Parts Per Million (PPM) v) Defect Level	10	CO1	BT2
7	a) Explain the following concepts related to system reliability and repair: i) Reliability ii) Failure Rate iii) Mean Time Between Failures (MTBF) iv) Mean Time To Repair (MTTR) v) System Availability b) Differentiate between functional testing, structural testing and exhaustive testing with respect to test generation, test application and fault detection.	10	CO1	BT2

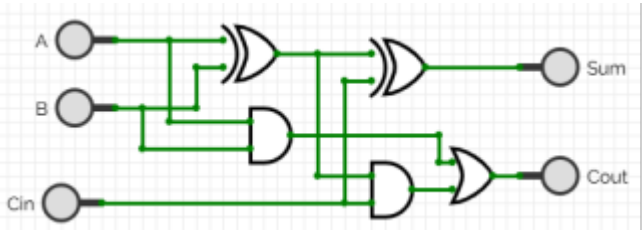
PART C: Answer Any 1 Following Questions. 10 M

Q.N.	Questions	M	CO	BT

8	a) For a two-input CMOS NOR gate, identify the possible transistor-level faults and develop the corresponding fault behavior/truth table. b) Explain the following bridging fault models with suitable diagrams: i) AND bridging fault ii) OR bridging fault iii) Dominant bridging fault v) Wired-AND and Wired-OR models	10	CO1	BT2
9	For the given circuit: i) Develop the Truth Table for Fault-Free and Faulty Circuits ii) Identify the Total Number of collapsed faults. 	10	CO1	BT2

PART D: Answer Any 1 Following Questions. 10 M				
Q.N.	**Questions**	**M**	**CO**	**BT**
10	For the given combinational circuit, calculate the SCOAP testability measures: i) CC0 – Controllability to logic 0 ii) CC1 – Controllability to logic 1 iii) CO – Observability Determine the testability of each internal node and identify the most difficult node to control and observe. 	10	CO2	BT3
11	For the given sequential circuit containing flip-flops and combinational logic, calculate the Sequential SCOAP measures. Determine: i) Sequential controllability of the specified nodes ii) Sequential observability of the specified nodes Show all intermediate calculations using the appropriate SCOAP equations. 	10	CO2	BT3

PART E: Answer Any 1 Following Questions. 10 M				
Q.N.	**Questions**	**M**	**CO**	**BT**

12	For the given combinational circuit consisting of AND, OR, NOT and NAND gates: i) Calculate CC0 and CC1 for all internal nodes. ii) Calculate the CO of the internal nodes. 	10	CO2	BT3
13	a) Explain the probability-based calculation of controllability for the following gates: i) NOT gate ii) AND gate iii) OR gate iv) NAND gate v) NOR gate b) For a two-input AND gate, assume independent input probabilities:P(A=1)=0.4,P(B=1)=0.7, Calculate: i) Probability of output being logic 1 ii) Probability of output being logic 0 iii) Compare the result with the corresponding SCOAP CC1 and CC0 measures.	10	CO2	BT3