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**Improving Computational Speed of the Multiplier Using Urdhva-Tiryagbhyam**

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**Abstract**

Multiplication is one of the commonly used arithmetic operations in digital electronics. In many complex operations, it forms the central factor such as filtering, Fast Fourier Transform (FFTs)Convolutions, etc.ALU is a digital processor is an essential block, as all computational operations are performed by this method. Multipliers so far are having large area, power, and delay. Due to this reason, an efficient multiplier with a concentrated area and high -speed performance is required. In this paper, a Vedic real multiplier based on as Urdhva-Tiryagbhyam sutra of Indian Vedic mathematics proposed. The main objective of this project is to provide an efficient 4\*4 multiplier, to implement a 4\*4 multiplier using Vedic sutra of mathematics “Urdhva-Tiryakbhyam” in FPGA and to decrease the area and delay path of a multiplier and increase the processor speed. The obtained result given by the proposed multiplier is better than the various multipliers in terms of area and speed. The algorithm is converted to code using Verilog and implemented on FPGA.

**Keywords:**

Vedic mathematics: Urdhva-Tiryakbhyam, Verilog, FPGA, FFTs.

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