Roll No												

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF INFORMATION SCIENCE

MID TERM EXAMINATION

Winter Semester: 2021 - 22

Course Code:

Course Name:

Program & Sem: SOIS & II

Date: 13/May/2022

Time: 01:30 PM – 03:00 PM

Max Marks: 50

Weightage: 25%

Instructions:

(i) Read the all questions carefully and answer accordingly.

Part A [Memory Recall Questions]

Answer all the Questions. Each question carries ONE mark. (1Qx10M=10M)

1. _____ register receives the data from memory to processor.

a. MAR b. MDR c.General Purpose Registers d. Instruction Register (C.O.No.1) [Comprehension]

2. SPEC in computer stands for _____.

a. Standard Performance Evaluation Corporation

b.System Evaluation Effective Corporation

c. Standard Performance Evaluation Computer

d.None of these (C.O.No.1) [Comprehension]

3. _____ refers to the act of converting programs written in high level programming language to low level language.

a. Assembler b. Processor c. Compiler d. Interpreter (C.O.No.1) [Comprehension]

4. _____ register will be used in the processor to store the next address of the instruction to get executed.

a. MAR b. MDR c.General Purpose Registers d. Program counter (C.O.No.1) [Comprehension]

5.Which statement is true about the bus?

a.Data bus transfers the data from processor to memory and vice versa.

b.Address bus transfer the address from processor to memory.

c.Control bus transfers read and write signals to the processor and memory.

d.All the above. (C.O.No.1) [Comprehension]

6. Which of the architecture is power efficient?

a. RISC b. ISA c. IANA d. CISC (C.O.No.1) [Comprehension]

7. To reduce the memory access time we generally make use of _____

a. SDRAM's b. Heaps c. Cache's d. Higher capacity RAM's (C.O.No.1) [Comprehension]

8. A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____

a. Super-scaling b. Pipe-lining c. Parallel Computation d. None of the mentioned

(C.O.No.1) [Comprehension]

9. CISC stands for _____

a. Complete Instruction Sequential Compilation
b. Computer Integrated Sequential Compiler
c. Complex Instruction Set Computer
d. Complex Instruction Sequential Compilation (C.O.No.1) [Comprehension]

10. The decoded instruction is stored in _____

a. IR b. PC c. Registers d. MDR (C.O.No.1) [Comprehension]

Part B [Thought Provoking Questions]

Answer all the Questions. Each question carries TEN marks. (2Qx10M=20M)

11. Consider a instruction Add A, B which is stored in memory. Explain how to transfer and process the data between the processor and memory with a neat block diagram.

(C.O.No.2) [Comprehension]

12. a) Indicate whether overflow occurs or not for the following given values

i) +8 & +15 ii) -12 & -2 (C.O.No.1) [Comprehension]

b) Demonstrate a n bit ripple carry adder by using Full Adder. (C.O.No.2) [Comprehension]

Part C [Problem Solving Questions]

Answer all the Questions. Each question carries TEN mark. (2Qx10M=20M)

13. Given A=18 and B=3 Apply Restoring Division and perform A/B (C.O.No. 3) [Application]

14. Apply Booth's Algorithm and multiply -13 & +9. (C.O.No. 3) [Application]

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PRESIDENCY UNIVERSITY
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SCHOOL OF INFORMATION SCIENCE

END TERM EXAMINATION

Winter Semester: 2021 - 22
Course Code: BCA 2017
Course Name: Computer Organization
Program & Sem: BCA – II Sem

Date: 1st July 2022
Time: 1:00PM to 04:00PM
Max Marks: 100
Weightage:50%

Instructions:

(i) Read the all questions carefully and answer accordingly.

Part A [Memory Recall Questions]

Answer all the Questions. Each question carries ONE marks. (20Qx 1M= 20M)

1. _____ register sends the address from processor to memory.
a. MDR b. MAR c.General Purpose Registers d. Instruction Register (C.O.No.1) [Comprehension]
2. SPEC in computer stands for _____.
a. Standard Performance Evaluation Corporation
b.System Evaluation Effective Corporation
c. Standard Performance Evaluation Computer
d.None of these (C.O.No.1) [Comprehension]
3. _____ refers to the act of converting programs written in Middle level programming language to low level language.
a. Assembler b. Processor c. Compiler d. Interpreter (C.O.No.1) [Comprehension]
4._____ register will be used in the processor to store the next address of the instruction to get executed.
a. MAR b. MDR c. General Purpose Registers d. Program counter (C.O.No.1) [Comprehension]
5.Which statement is not true about the bus?
a. Control bus transfers read and write signals to the processor and memory.
b.Address bus transfer the address from processor to memory.
c. Data bus transfers the data only from processor to memory and not from memory to Processor.
d.All the above. (C.O.No.1) [Comprehension]
6. Which of the architecture is power efficient?
a. ISA b. RISC c. IANA d. CISC (C.O.No.1) [Comprehension]
7. To reduce the memory access time we generally make use of _____
a. SDRAM's b. Heaps c. Cache's d. Higher capacity RAM's (C.O.No.1) [Comprehension]
8. A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____
a. Super-scaling b. Pipe-lining c. Parallel Computation d. None of the mentioned
(C.O.No.1) [Comprehension]
9. RISC stands for _____
a. Reduced Instruction Sequential Compilation

b. Reduced Integrated Sequential Compiler
c. Reduced Instruction Set Computer
d. Reduced Instruction Sequential Compilation (C.O.No.1) [Comprehension]
10. The decoded instruction is stored in _____
a. IR b. PC c. Registers d. MDR (C.O.No.1) [Comprehension]
11. _____ register receives the data from memory to processor.
a. MAR b. MDR c.General Purpose Registers d. Instruction Register (C.O.No.1) [Comprehension]
12. What is the high speed memory between the main memory and the CPU called?
a. Register Memory b. Cache Memory c. Storage Memory d. Virtual Memory
(C.O.No.3) [Comprehension]
13. _____ refers to the act of converting programs written in high level programming language to low level language.
a. Assembler b. Processor c. Compiler d. Interpreter (C.O.No.1) [Comprehension]
14. _____ register will be used in the processor to store the next address of the instruction to get executed.
a. MAR b. MDR c. General Purpose Registers d. Program counter (C.O.No.1) [Comprehension]
15. Whenever the data is found in the cache memory it is called as _____
a. HIT b. MISS c. FOUND d. ERROR (C.O.No.4) [Comprehension]
16. In _____ mapping, the data can be mapped anywhere in the Cache Memory.
a. Associative b. Direct c. Set Associative d. Indirect (C.O.No.3) [Comprehension]
17. The transparent register/s is/are _____
a. Y b. Z c. Temp d. All of the mentioned (C.O.No.3) [Comprehension]
18. . _____ signal is used to show complete of memory operation.
a. WFC b. WMFC c. CFC d. None of the mentioned (C.O.No.3) [Comprehension]
19. CISC stands for _____
a. Complete Instruction Sequential Compilation
b. Computer Integrated Sequential Compiler
c. Complex Instruction Set Computer
d. Complex Instruction Sequential Compilation (C.O.No.1) [Comprehension]
20. The main advantage of multiple bus organisation over a single bus is _____
a. Reduction in the number of cycles for execution b. Increase in size of the registers
c. Better Connectivity d. None of the mentioned (C.O.No.4) [Comprehension]

Part B [Thought Provoking Questions]

Answer all the Questions. Each question carries 10 marks. (4Qx10M=40M)

21. Consider a instruction Add A, B which is stored in memory. How to transfer and process the data between the processor and memory with a neat block diagram. (C.O.No.2) [Comprehension]
22. Discuss one address, Two address and Three address Instructions for the given expression C→(A+B)*(C+D) . (C.O.No.2) [Comprehension]
23.Define Bus Arbitration. With a neat block diagram demonstrate different types of bus arbitration. (C.O.No.4) [Comprehension]
24.How data will be transferred from keyboard to monitor in program controlled I/O communication. (C.O.No.4) [Comprehension]

Part C [Problem Solving Questions]

Answer all the Questions. Each question carries 10 marks. (2Qx20M=40M)

25. Apply Booth's Algorithm and multiply -13 & +9. (C.O.No. 3) [Application]
26.Illustrate single bus Organization and also demonstrate the different steps for the code ADD (R1),R2 by using execution of the complete instructions. (C.O.No.4) [Comprehension]