PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

TEST 1

Winter Semester: 2021 - 22

Course Code: CSE 2009

Course Name: Computer Organization and Architecture

Program & Sem: B-Tech & IV Semester

Date:

Time:

Max Marks: 30

Weightage: 15 %

Instructions:

(i) Read the all questions carefully and answer accordingly.
(ii) Question paper consists of 3 parts.
(iii) Scientific and Non-programmable calculators are permitted.

Part A [Memory Recall Questions]

Answer all the Questions. Each question carries TWO marks. (3Qx 2M = 6M)

1. Define Memory Access Time. [2] (C.O.No.1) [Knowledge Level]
2. Discuss the functional units of a computer. [2] (C.O.No.1) [Knowledge Level]
3.. Discuss the usages of at least four special purpose processor registers.

[2] (C.O.No.1) [Knowledge Level]

Part B [Thought Provoking Questions]

Answer all the Questions. Each question carries FOUR marks. (3Qx4M = 12M)

4. Consider a 64-bit machine where an instruction (LOAD R3, [M]) is stored at memory location 6024. Discuss the contents of registers IR, MAR, MDR while the instruction is being fetched?

[4] (C.O.No.1) [Comprehension Level]

5. Distinguish between CISC and RISC family of processors with relevant examples.

[4] (C.O.No.1) [Comprehension Level]

6. Summarize the advantages of 2's complement representation over the other schemes

[4] (C.O.No.1) [Comprehension Level]

Part C [Problem Solving Questions]

Answer both the Questions. Each question carries SIX marks. (2Qx6M = 12M)

7. A program contains 1000 instructions. Out of that 50% instructions are in straight line code and the remaining are in a loop that executes 10 times. The average number of basic steps needed to execute one machine instruction is 2 cycles and the processor is controlled by a clock of 2GHz. Find the time required for the program execution. [6] (C.O.No.1) [Application Level]

8. Represent the following pairs of signed decimal numbers in 4 bit 2's complement numbers and add them. State whether overflow occurs or not.

i) +2 and +3

ii) +4 and +5

iii) +7 and -3

[6] (C.O.No.1) [Application Level]

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TEST 2

Winter Semester: 2021 - 22

Course Code: CSE 2009

Course Name: Computer Organization and Architecture

Program & Sem: B-Tech & 4th Semester

Date:1st June 2022

Time: 11:30 am to 12:30 pm

Max Marks: 30

Weightage: 15 %

Instructions:

(i)   Read the all questions carefully and answer accordingly.

(ii) Question paper consists of 3 parts.

(iii) Scientific and Non-programmable calculators are permitted.

Part A [Memory Recall Questions]

Answer all the Questions. Each question carries Four marks.   (3Qx 4M = 12M)

1. Define a Full adder with its truth table and write the logic expression for Sum and Carry.

(C.O.No.2)[Knowledge Level]

2. With an example, discuss two address and one address instruction formats.

(C.O.No.1) [Knowledge Level]

3. With suitable diagram explain the two types of Byte Addressability?

(C.O.No.1) [Knowledge Level]

Part B [Thought Provoking Questions]

Answer the following question. The question carries Eight marks.   (1Qx8M = 8M)

4. In Ripple Carry Adder, each full adder has to wait for its carry-in from its previous stage full adder. Thus, nth full adder has to wait until all (n-1) full adders have completed their operations. This causes a delay and makes ripple carry adder extremely slow. The situation becomes worst when the value of n becomes very large. Can we overcome this disadvantage? If yes, explain the process in detail with relevant proofs.

(C.O.No.2) [Comprehension Level]

Part C [Problem Solving Questions]

Answer all the Question. Each question carries Five marks.   (2Qx5M = 10M)

7. Register R1 and R2 of computer contain the decimal value 1800 and 2600 respectively. What is the effective address of the source operand in each of the following instructions? (Assume 32-bit word length)   (C.O.No.1) [Application Level]

    (i) Load 20(R1), R2

    (ii) Move #3000, R4

    (iii) Store 30(R1, R2), R4

    (iv) Add –(R2), R4

    (v) Subtract (R1)+, R4

    (vi) Mov (R1, R2), R4

    (vii) ADD 100(R1, R2), R4

8. What is the purpose of a stack pointer. Assume 32-bit word length memory, Stack Pointer is initially loaded with address value 4800. After performing a push operation what will be the location of the item pushed onto the stack? Also write the instruction to implement a PUSH operation.

(C.O.No.1) [Application Level]

PRESIDENCY UNIVERSITY
BENGALURU

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

SCHOOL OF MANAGEMENT

END TERM EXAMINATION

Winter Semester: 2021 - 22

Course Code: CSE 2009

Course Name: Computer Organization and Architecture

Program & Sem: B. Tech & IV Sem

Date: 28th June 2022

Time: 09:30 AM to 12:30 PM

Max Marks: 100

Weightage: 50%

Instructions:
 (iv) Read the all questions carefully and answer accordingly.
 (v) Answers should be precise.

Part A [Memory Recall Questions]

Answer all the Questions. Each question carries FIVE marks.   (6Qx 5M=30M)

1. Describe CALL and RETURN instructions in Subroutines.   (C.O.No.1) [Knowledge]
2. Define the working principle of a processor stack. Explain the implementation of PUSH and POP Operations.   (C.O.No.1) [Knowledge]
3. State the difference between two address and one address instruction formats with example.   (C.O.No.1) [Knowledge]
4. Briefly describe the special purpose registers present in a processor.   (C.O.No.1) [Knowledge]
5. Define Cache mapping techniques, name the three types.   (C.O.No.1) [Knowledge]
6. Discuss the concept of Effective Address with relevant example.   (C.O.No.1) [Knowledge]

Part B [Thought Provoking Questions]

Answer all the Questions. Each question carries EIGHT marks.   (5Qx8M=40M)

7. Explain the steps to handle Interrupts with a relevant diagram.   (C.O.No.1) [Comprehension]
8. Discriminate between the following: (C.O.No.2) [Comprehension]
 i) Polling and Interrupt driven I/O   ii) Memory mapped I/O and I/O mapped I/O.
9. With a neat diagram explain the Single bus Organization of a BPU. (C.O.No.3) [Comprehension]
10. An element cannot be popped out from an empty stack, similarly one cannot push any element into a stack that is full. Discuss the instructions to safely push and pop in a stack taking care of these conditions.   (C.O.No.2) [Comprehension]
11. Explain the internal organization of 128*16 Memory chip. State the external connections are required for the chip.   (C.O.No.3) [Comprehension]

Part C [Problem Solving Questions]

Answer both the Questions. Each question carries FIFTEEN marks.   (2Qx15M=30M)

12. Write a flowchart for the non-restoring division algorithm.
    Given A = 13 and B = 5 perform A/B using restoring division algorithm.   (C.O.No.3) [Application]
13. Explain Booth's Multiplication algorithm. Apply booth algorithm to multiply the signed integers +10 and -6.   (C.O.No.3) [Application]