Roll No												

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

TEST-1 EXAMINATION

Fall Semester: 2021 - 22

Course Code: ECE 2002

Course Name: Digital Electronics

Program & Sem: B. Tech. & 4th Semester

Date: 27/04/2022

Time: 11:30 AM to 12:30 PM

Max Marks: 30

Weightage: 15%

Instructions:

(i) Read the all questions carefully and answer accordingly.
(ii) Draw diagrams wherever necessary.
(iii) Use of non-programmable scientific calculator is permitted.

Part A [Memory Recall Questions]

Answer all the Questions. Each question carries one mark. (12Qx 1M= 12M)

1) 2's compliment is used for representing signed number. What is correct representation of -45 in 8 bit 2 complement form? [01 M] (C.O.No.1) [Knowledge]

2) The 10's complement is also used to find the subtraction of the decimal numbers. What is the 10's complement of 782.54? [01 M] (C.O.No.1) [Knowledge]

3) The logic gates are classified into three different categories. NAND & NOR GATE are belongs to _____ category. [01 M] (C.O.No.2) [Knowledge]

4 There are 16 input combinations in the truth table of digital system. State the number of input variables required for framing a Standard form Boolean expression? [01 M] (C.O.No.2) [Knowledge]

5) In order to communicate, we need not only numbers but also letters of alphabet, punctuation marks and other special character .These codes are called as _____. [01 M] (C.O.No.2) [Knowledge]

6] There are four possible combinations of inputs in truth table of NAND gate. What is the value of output when one input out of two goes low. [01 M] (C.O.No.2) [Knowledge]

7] A number expressed in the binary numeral system is odd if its last digit is 1. Which logic gate generates a HIGH output when an odd number of inputs are HIGH? [01 M] (C.O.No.2) [Knowledge]

8] The hexadecimal numeral system is a positional numeral system that represents numbers using a radix (base) of 16. The decimal equivalent of $(159)_{16}$ [01 M] (C.O.No.2) [Knowledge]

9] The Boolean algebra specifies various laws for simplification of logic expression. The Boolean law A' + B' + C'=(A · B · C)' is also known as_____ Law.

[01 M] (C.O.No.2) [Knowledge]

10] Along with binary numbers binary codes are also used for digital design. BCD is Binary Coded Decimal code. BCD is also called as _____ code. [01 M] (C.O.No.2) [Knowledge]

11] Similar to decimal fractions, binary numbers can also be represented as unsigned fractional numbers by placing the binary digits to the right of the decimal point or in this case, binary point. In the binary number 1110.1010, the fractional part has the value.

[01 M] (C.O.No.2) [Knowledge]

12] The excess-3 code is a non-weighted code used to express code used to express decimal numbers. The excess -3 code equivalent for 5 is _____. [01 M] (C.O.No.2) [Knowledge]

Part B [Thought Provoking Questions]

Answer all the Questions. Each question carries four marks. (3Qx4M=12M)

13) SOP and POS are the two types of representations in digital design. As a designer of digital circuit, which representation you will prefer? Justify your design choice.

[04 M] (C.O.No.2) [Comprehension]

14) An integrated circuit (IC) is a set of electronic circuits on one small flat piece (or "chip") of semiconductor material, usually silicon. ICs have two main advantages over discrete circuits: cost and performance. Logic gates are available as ICs. Mr. Antony is provided with Boolean function (x'.y'.z' + x'.y.z + x.y.z + x'.y.z').

i) As a designer, estimate the number of basic gate ICs are required to implement given expression.

ii) Develop truth table for the given expression. [04 M] (C.O.No.2) [Comprehension]

15) The digital system designer has been given with task of designing digital circuit from Boolean expression. The simplification of given equation is an inevitable step in this process. Which method among the two (K-map and Boolean algebra), you will prefer for simplification of expression? Justify your answer with suitable example. [04 M] (C.O.No.2) [Comprehension]

Part C [Problem Solving Questions]

Answer the Question. Question carries twelve marks. (1Qx06M=06M)

16) In Boolean algebra, circuit minimization is the problem of obtaining the smallest logic circuit that represents a given Boolean function or truth table. Mr. Joel is provided with Boolean function F=∑m(0,1,3,4,6,7,8,9,11,12,14,15). For designing the Boolean function into digital circuits, he has to simplify the function using K-map.

(i) How many product term are present in the simplified function. Write expression obtained from K-map.

(ii) How many no of TWO input basic gates are needed for implementation of given expression?

(iii) Give your remarks on how gate level minimization with help Mr. Joel.

[06 M] (C.O. No. 2) [Application]

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GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

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TEST 2

Winter Semester: 2021 - 22
Course Code: ECE 2002
Course Name: Digital Electronics
Program & Sem: B. Tech & IV Sem

Date: 2ND JUNE 2022
Time: 11:30 AM to 12:30 PM
Max Marks: 30
Weightage: 15%

Instructions:

(i) Read the all questions carefully and answer accordingly.

Part A [Memory Recall Questions]

Answer all the Questions. Each question carries TWO marks. (4Qx 2M= 8M)

1. An Decoder is a combinational logic circuit; it decodes certain set of inputs to outputs. In N: 2^N decoder the OUTPUT has ____bit binary form. **(C.O.No.3) [Knowledge]**

2. An adder is a combinational logic circuit whose output are sum and carry. If two numbers, $(6)_{10}$ and $(7)_{10}$ are added using a full adder. At LSB position of both the numbers, _____ will be the sum ----and _____ will be the carry. **(C.O.No.3) [Knowledge]**

3. The outputs of a comparator irrespective of number of bits are _____, _____ and _____.

(C.O.No.3) [Knowledge]

4. Multiplexer (MUX) is a Combinational logic circuit having single output line and manyinput lines. On the basis of select lines, one of the input lines is transferred to output line. Write the Boolean expression for the output of the 4:1 MUX**.** **(C.O.No.3) [Knowledge]**

Part B [Thought Provoking Questions]

Answer ANY questions. Each question carries FOUR marks. (3Qx4M=12M)

5. Higher order Multiplexer (MUX) can be implemented using lower order MUX by providing the output of the lower MUX to the input of the next MUX. Design higher order MUX (8 x 1) using (2 x 1) MUX and how many (2 x 1) MUX is required to implement (8 x 1) MUX.

(C.O.No. 3) [Comprehension]

6. To compare numbers, Magnitude comparator is used. Develop and report a 1-Bit comparator with the final Boolean expressions for all the outputs of comparator. **(C.O.No. 3) [Comprehension]**

7. Mr. Joy is working on a combinational circuit which will convert binary into octal. Suggest a suitable circuit for the required conversion and draw the circuit diagram using basic gates only**.**

(C.O.No. 3) [Comprehension]

8. To obtain minimized Boolean expression from Boolean function, K-Map is one of the methods. In the given condition, obtain minterms in the Product-of-Sum form and function is given as *F* (*A*, *B*, *C*, *D*) = π((1, 3, 5, 7, 13, 15). **(C.O.No. 2) [Comprehension]**

Part C [Problem Solving Questions]

Answer ANY ONE Question. Each question carries TEN marks. (1Qx10M=10M)

9. A digital logic switching function is described by the following Boolean Function in SOP. Simplify the function using Quine Mc Cluskey Method and obtain essential prime-implicants F(A,B,C,D)=∑(0,1,3,7,8,9,11,15) . **(C.O.No. 2) [Application]**

10.Implement F(A,B,C,D)=∑m(0,2,3,5,6,7,8,9,12,13) Using MUX (Variable Entered Method)(VEM). **(C.O.No. 3) [Application]**

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END TERM Examination

EVEN Semester: 2022-23
Course Code: ECE 2002
Course Name: Digital Electronics
Program & Sem: B. Tech & IV Sem

Date: 30th June 2022
Time: 9:30 AM to 12:30 PM
Max Marks: 100
Weightage: 50%

Instructions:

(iv) Read Questions carefully and answer accordingly
(v) Scientific and Non- programmable calculators are permitted

PART A (Memory Recall Questions)

Answer all the questions. **Each question carries TWO Marks**. **[15Q x 2M = 30M]**

Q1. For designing a 4 bit Asynchronous counter how many JK flipflop are required? Which input condition of JKFF is used to Asynchronous design counter. [CO4 B. Level:Knowledge]

Q2.T –flip flop is modified version of ----------Flip flop , In T-flip flop ,for what input combinations it produces no change state? [CO4 B. Level:Knowledge]

Q3. Logic gates are the basic building blocks of any digital system. It is an electronic circuit having one or more than one input and only one output. Identify the gate whose output goes High if only any one of the inputs are zero? [CO1 B. Level: Knowledge]

Q4. In Priority Encoder, D0,D1 & D2 are high means what is the encoded value of a 8 into 3 line Encoder ? [CO3 B. Level: Knowledge]

Q5. Which flipflop is called as transparent flip flop? , Write its characteristic equation. [CO4 B. Level: Knowledge]

Q6. Match the following and choose the correct option:

a. Octal to binary converter	1. Sequential circuit
b. 4-to-1 MUX	2. Universal gate
c. 4 bit counter	3. 3:8 encoder
d. NOR gate	4. Combination circuit
e. Full adder	5. Half adders, OR gate

[2Mx5Q][CO1,2, 3,4 B. Level: Knowledge]

Q7. A _____ logic circuits depends only on the present inputs ,not on previous output. And it does not have memory and no feedback element. Give an example for the same. (CO.2) [B. Level: Knowledge]

Q8. In Carry look Ahead Adder , there are Generate function and Propagate function which are expressed as _____ and_____. (CO.3) [B. Level: Knowledge]

Q9.A Multiplexers are used in various applications where in multiple-data need to be transmitted by using a single line. In an Communication System application it uses multiplexers 32:1 MUX for signal transmission which has _____inputs ,_____output & _____selection lines. (CO.3) [B. Level: Knowledge]

Q10 .If the input to 3 bit Binary to Gray converter is 111 then the expected output is_____. (CO.1) [B. Level: Knowledge]

Q11. An adder is a combinational logic circuit whose output are sum and carry. If two numbers, $(13)_{10}$ and $(15)_{10}$ are added using a full adder. At LSB position of both the numbers, _____ will be the sum ----and _____ will be the carry. (CO.1) [B. Level: Knowledge]

PART B (Thought Provoking Questions)

Answer any FIVE Questions. Each Question carries EIGHT Marks. **[5Q x 8M = 40M]**

Q12 .Roy and his friends are interested to design a block that has 1 input line and 16-bit output and that block is named as De-Multiplexer that performs reverse operation of a Multiplexer. Help them to build the block but they have only 1:2 DEMUX. Hence, implement 1:16 DEMUX using 1:2 DEMUX.
[CO3 B. Level: Comprehension]

Q13. Full Adder is the adder which adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM

i. Implement the full adder using the minimum no of logical gates.
ii. A decoder is a device that generates the original signal as output from the coded input signal and converts n lines of input into 2^n lines of output. Interpret full adder using 3 to 8 decoder. [CO3 B. Level: Comprehension]

Q14.Mr JOY wants to implement a warning buzzer when the following conditions apply:

- Switches A, B, C are on.
- Switches A and B are on but switch C is off
- Switches A and C are on but switch B is off.
- Switches C and B are on but switch A is off.

Draw a truth table for this situation and obtain a Boolean expression for it.Minimize this expression and draw a logic diagram using NAND GATES.
[CO3 B. Level: Comprehension]

Q15. Asynchronous counter in which output of system clock is applied as clock signal only to first flip flop. The remaining flip-flops receive the clock signal from output of its previous stage flipflop. Hence, the outputs of all flip-flops do not change affect at the same time. Design 3-bit Asynchronous counter using T-FlipFlop. Draw the truth table & waveform of counter o/p.
[CO3 B. Level: Comprehension]

Q16. A comparator is a device that compares two bits, voltage or currents and outputs a digital signal indicating which is larger. Design a 2-Bit comparator with the help of truth table and obtain the logical expression for each case with the help of simplification method (K-map).
[CO3 B. Level: Comprehension]

Q17.Explain with the help of Truth table ,characteristic table ,excitation table, obtain the characteristic equation, excitation equation and also draw the logical diagram using NAND gate for JKFF. [CO3 B. Level: Comprehension]

PART C (Problem Solving Questions)

Answer any THREE the Questions. Each Question carries TEN Marks. **[3Q x 10M = 30M]**

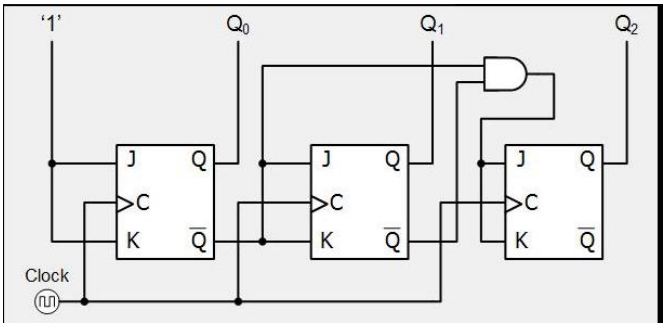
Q18. To count the number of clocks a circuit had be developed. So, to perform 3-Bit counting Flip flop based circuit has to be developed. Choose the appropriate Flip flop required and design the circuit so that the resultant will be a synchronous UP counter. To support the design, draw the truth table/ excitation table. (C.O.No. 4) [Application]

Q19. A digital logic switching function is described by the following Boolean Function in SOP. Simplify the function using Quine Mc Cluskey Method and obtain essential prime-implicants

F(A,B,C,D)=∑(0,5,7,8,9,10,11,14,15) . (C.O.No. 2) [Application]

Q20. Designing a sequential circuit involves the representation of sequential circuit models. It includes a state diagram, state table, reduced state table, reduced state diagram. The logic diagram is given below for which, obtain:(J0,K0, J1,K1,J2,K2 ,Q0,Q1,Q2 are respectively inputs and outputs w.r.t the below diagram)

a. State equations
b. State Table
c. State Diagram.



[3M+5M+2M] (C.O.No. 4) [Application]

Q21. A digital system is to be designed in which the month of the year is given as input is four bit form. The month January is represented as '0000', February '0001' and so on. The output of the system should be '1' corresponding to the input of the month containing 31 days or otherwise it is '0'. Consider the excess numbers in the input beyond '1011' as don't care conditions for system of four variables (A, B, C, D).

i) Design and implement the simplified logic using LOGICAL GATES.
ii) Design and implement the simplified logic using 8:1 MUX.

[10 M] (C.O.No. 1) [Application]