## PRESIDENCY UNIVERSITY

BENGALURU

## SCHOOL OF ENGINEERING

## MID TERM EXAMINATION

Winter Semester: 2021-22
Course Code: ECE 2007
Course Name: Digital Design
Program \& Sem: B. Tech \& 2 ${ }^{\text {nd }}$ Semester

Date: 12/MAY/2022
Time: 01:30 PM - 03:00 PM
Max Marks: 50
Weightage: 25\%

## Instructions:

(i) Read the all questions carefully and answer accordingly.
(ii) Draw diagrams wherever necessary.
(iii) Use of non-programmable scientific calculator is permitted.
(iv) Total Question is 12.

## Part A [Memory Recall Questions]

Answer all the Questions. Each question carries ONE marks.

Match the following.

| 1 | Decimal Equivalent of (AC2) $1_{6}$ | a | $(A+B)(A+C)$ |
| :---: | :---: | :---: | :---: |
| 2 |  | b | $\begin{aligned} & A-9 \\ & B-\mathrm{OUT} \\ & \hline \end{aligned}$ |
| 3 | $A+B C$ | C | 234 |
| 4 |  | d |  |
| 5 | $\overline{\overline{(A+B)}+\bar{C}}$ | e | 2754 |
| 6 | Decimal Equivalent of (11101010)2 | f | ( $\mathrm{A}+\mathrm{B}$ ) C |

7. Similar to decimal fractions, binary numbers can also be represented as unsigned fractional numbers by placing the binary digits to the right of the decimal point or in this case, binary point. In the binary number 1100.0101, the fractional part has the value $\qquad$ .
(C.O.No.1) [Knowledge Level]
8. A digital input detects if a voltage is above/below a specific threshold. How many different sets of input conditions will produce a HIGH output from a five-input OR gate?
(C.O.No.1) [Knowledge Level]
9. The implementation of Boolean functions by using logic gates involves connecting output of one logic gate to the input of another gate. Logic Gates are the basic building blocks of digital electronic circuits. The number of basic gates required to implement the expression $F=x^{\prime}+y^{\prime} z$ is
$\qquad$ -.
(C.O.No.1)[Knowledge Level]
10. There are four main types of number systems - Binary, decimal, hexadecimal and octal. The hexadecimal equivalent of given binary system $(1010000.0001)_{2}$ is $\qquad$ .
(C.O.No.1) [Knowledge Level]
11. AND-OR-Invertor (AOI) logic, is mostly used for all design of circuit. For example, if a person has to design AOI logic using a single type of gate that gives HIGH output when both the inputs are LOW. Realise all 3 gates based on the given condition. (C.O.No.1) [Knowledge Level]
12. NAND gate is used mostly for sum of product circuit implementation. The canonical sum of product form of the function $y(A, B)=A+B$ is $\qquad$ . (C.O.No.1) [Knowledge Level]

## Part B [Thought Provoking Questions]

Answer all the Questions. Each question carries SIX mark.
$(3 Q \times 6 M=18 M)$
13. A table is used to represent the Boolean expression of a logic gates function is called the logic gates. A logic gates truth table shows each possible input combination to the circuit with the resultant output depending upon the combination of the inputs.
(a) Find the Boolean expression in the standard sum of product (SOP) from the given truth table.
(b) Simplify the expression and implement (draw) using logic gates.

| Inputs |  |  | Outputs |
| :---: | :---: | :---: | :---: |
| $X$ | $Y$ | $Z$ | $F$ |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

$(2+2+2=6)$
(C.O. No-1) [Application Level]
14. In a certain chemical-processing plant, a liquid chemical is used in a manufacturing process. The chemical is stored in three different tanks. A level sensor in each tank produces a HIGH voltage when the level of chemical in the tank drops below a specified point.
Design and implement a circuit using AND-OR-NOT (AOI) logic that monitors the chemical level in each tank and indicates the level in any two of the tanks drops below the specific point.
(C.O. No-1, 2) [Application Level]
15. The digital system designer has a task to design the digital circuit. The circuit given below is the part of the very large digital circuit system. Use the given circuit and find the output expression of the given circuit.
(3+3=6 M) (C.O. No-1, 2) [Application Level]
(a)

(a)
(b)

(b)

## Part C [Problem Solving Questions]

Answer all the Questions. Each question carries TEN marks.
(2Qx10M=20M)
16. A combinational circuit is a type of a digital logic which is implemented by the Boolean expression circuits where the output is a pure function of a present inputs only. Half adder is such a combinational circuit which add two one-bit binary number.
(a) Draw the truth table of the half adder and implement the same using XOR and basic gates.
(b) Design and the full adder logic circuit using half adder circuits.
(10 marks) (C.O.No-2)[Application Level]
17. The K-Map (Karnaugh Map) is a method of simplifying Boolean expression. Maurice Karnaugh introduces this method in year 1953. K-Map can take two forms Sum of products (SOP) and Product of Sum (POS) according to the need of the problem. Don't care denotes inputs that are invalid for a given digital circuit. Thus, they can used to further simplify the Boolean output expression of a digital circuit. Don't care also prevents hazards in digital systems.
(a) Using the concept of the K-Map and don't care minimise the below given Boolean function in SOP minimal from using K-Map.

$$
F(A, B, C, D)=\sum m(1,2,6,7,8,13,14,15)+d(0,3,5,12)
$$

(b) Implement (draw) the simplified form using logic gates and tell the number of one input or two inputs logic gates required to implement.
(c) Comment why there is a need of minimisation in Boolean expression.

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MID-TERM EXAMINATION

Winter Semester: 2021-22
Course Code: ECE2007
Course Name: Digital Design
Program \& Sem: B. Tech \& 2 ${ }^{\text {nd }}$ Semester

Date: 29/06/2022
Time: 01:00PM - 04:00PM
Max Marks: 100
Weightage: 50\%

## Instructions:

(v) Read the all questions carefully and answer accordingly.
(vi) Draw diagrams wherever necessary.
(vii) Use of a non-programmable scientific calculator is permitted.

## Part A [Memory Recall Questions]

Answer all the Questions. Each question carries TWO marks.
(15Q $\times 2 \mathrm{M}=30 \mathrm{M})$

1. Many applications (eg: electromechanical switches and digital communication) require minimization of errors to prevent spurious outputs. In such cases, THE ------CODE IS used for its minimal changes in bits between two numbers.
(CO1, Knowledge)
2. Digital circuits can be broadly classified as Combinational circuits, and Sequential circuits. In a combinational circuit, the output depends on $\qquad$ (CO1, Knowledge)
3. Multiplexer are combinational circuit which has certain input and output lines. In addition to this, other input signals are present in MUX design called select lines. A 16:1 MUX has $\qquad$ inputs,
$\qquad$ output\& $\qquad$ selection lines:
(CO1, Knowledge)
4. A half adder can be constructed by using some logic gates which perform an operation of adding two binary digits. It produces two outputs Sum and Carry. Which logic gates can be used to implement its two outputs?
(CO1, Knowledge)
5. In the designing of Synchronous Counter, the circuit operation is controlled by (CO1, Knowledge)
6. When a level-triggered latch is enabled, it becomes transparent, but an edge-triggered flip-flop's output only changes on a single type (positive going or negative going) of clock edge. Which flipflop is called a transparent flipflop and write its characteristic equation.
(CO1, Knowledge)
7. Flip flop is a circuit element where the output depends on the present inputs and the former input and outputs. Which of the following input combinations is not allowed in an SR flip-flop? (CO1, Knowledge)
8. A Counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. For designing a N bit synchronous counter, we need how many D flipflop?
(CO1, Knowledge)
9. JK flip-flop is a controlled Bi-stable latch where the clock signal is the control signal. Thus, the output has two stable states based on the inputs. In JK flipflop which input combinations produce SET state?
(CO1, Knowledge)
10. A combinational logic circuit is a circuit whose outputs depends only on the current state of its inputs. Which device has many inputs and one output?
(CO1, Knowledge)
11. The binary number system and digital codes are fundamental to computers and digital electronics. Convert the decimal number (47.32) ${ }_{10}$ to binary and hexadecimal number systems.
(CO1, Knowledge)
12. Apply DeMorgan's theorems to each of the following expressions:

$$
\overline{(A+B+C) D}
$$

(CO1, Knowledge)
13. Simplify the following Boolean expression:

$$
\overline{A B+A C}+\bar{A} \bar{B} C
$$

(CO1, Knowledge)
14. AND-OR-Invertor (AOI) logic, is mostly used for all design of circuit. For example, if a person has to design AOI logic using a single type of gate that gives HIGH output when both the inputs are equal. Realise gates based on the given condition. Write its name, truth table and Boolean expression for the realized gate.
(CO1, Knowledge)
15. A half subtractor can be constructed by using some logic gates which performs operation of subtracting two binary digits. Subtract the LSB of (6) $)_{10}-(7)_{10}$.
(CO1, Knowledge)

## Part B [Thought Provoking Questions]

## Answer all Questions. Each question carries TEN marks.

(4Q $\times 10 \mathrm{M}=40 \mathrm{M}$ )
16. A decoder is a circuit that changes a code into a set of signals. A decoder is a digital circuit that detects the presence of a specified combination of bits (code) on its inputs and indicates the presence of that code by a specified output level.
(a) Design the $3 \times 8$ decoder with the $2 \times 4$ decoder.
(b) Using $3 \times 8$ decoder, implement the full adder circuit.
(5+5=10 M) (C.O. No-1, 2) [Application Level]
17. The term asynchronous refers to events that do not have a fixed time relationship with each other. An asynchronous counter is one in which the flip-flops (FF) within the counter do not change states simultaneously because they do not have a common clock pulse.
Design the 3-bit asynchronous UP counter with the T flipflop and explain its working.
(10 M) (C.O. No-1, 2) [Application Level]
18. The basic function of a comparator is to compare the magnitudes of two binary quantities to determine the relationship of those quantities. Design the 2-bit comparator and implement it using logic groups.
(10 M) (C.O. No-1, 2) [Application Level]
19. A table is used to represent the Boolean expression of a logic gates function is called the logic gates. A logic gates truth table shows each possible input combination to the circuit with the resultant output depending upon the combination of the inputs.
(c) Find the Boolean expression in the standard sum of product (SOP) from the given truth table and simplify the expression using KMap.
(d) Implement the standard SOP with 4:1 MUX.

| Inputs |  |  | Outputs |
| :---: | :---: | :---: | :---: |
| $X$ | $Y$ | $Z$ | $F$ |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

(5+5=10 M) (C.O. No-1) [Application Level]

## Part C [Problem Solving Questions]

Answer any Three Questions. Each question carries FIFTEEN marks.
(2Q $\times 15 \mathrm{M}=30 \mathrm{M}$ )
20. JK flip-flop is a controlled Bi-stable latch where the clock signal is the control signal. Thus, the output has two stable states based on the inputs. Draw the logic symbol and circuit diagram with the appropriate JK and T flip flop truth table. Derive the characteristic equation of JK and T flip flop.
(7.5+7.5=15 M) (C.O.No-2)[Application Level]
21. A synchronous counter is one in which all the flip-flops in the counter are clocked at the same time by a common clock pulse. Using the concept of clock synchronization to design the 3 -bit synchronous UP counter, explaining all the steps.
(15 M) (C.O. No-1, 2) [Application Level]

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## Instructions:

(viii) Read the all questions carefully and answer accordingly.
(ix) Draw diagrams wherever necessary.
(x) Use of non-programmable scientific calculator is permitted.
(xi) Total Question is 12.

## Part A [Memory Recall Questions]

Answer all the Questions. Each question carries ONE marks.

Match the following.

| 1 | Decimal Equivalent of (AC2) $1_{6}$ | a | $(A+B)(A+C)$ |
| :---: | :---: | :---: | :---: |
| 2 |  | b | $\begin{aligned} & A-9 \\ & B-\mathrm{O} \\ & \hline \end{aligned}$ |
| 3 | $A+B C$ | C | 234 |
| 4 | $A \rightarrow 0-\text { out }$ | d |  |
| 5 | $\overline{\overline{(A+B)}+\bar{C}}$ | e | 2754 |
| 6 | Decimal Equivalent of $(11101010)_{2}$ | f | (A+B) C |

18. Similar to decimal fractions, binary numbers can also be represented as unsigned fractional numbers by placing the binary digits to the right of the decimal point or in this case, binary point. In the binary number 1100.0101, the fractional part has the value $\qquad$ .
(C.O.No.1) [Knowledge Level]
19. A digital input detects if a voltage is above/below a specific threshold. How many different sets of input conditions will produce a HIGH output from a five-input OR gate?
(C.O.No.1) [Knowledge Level]
20. The implementation of Boolean functions by using logic gates involves connecting output of one logic gate to the input of another gate. Logic Gates are the basic building blocks of digital electronic circuits. The number of basic gates required to implement the expression $F=x^{\prime}+y^{\prime} z$ is
$\qquad$ .
(C.O.No.1)[Knowledge Level]
21. There are four main types of number systems - Binary, decimal, hexadecimal and octal. The hexadecimal equivalent of given binary system $(1010000.0001)_{2}$ is $\qquad$ .
(C.O.No.1) [Knowledge Level]
22. AND-OR-Invertor (AOI) logic, is mostly used for all design of circuit. For example, if a person has to design AOI logic using a single type of gate that gives HIGH output when both the inputs are LOW. Realise all 3 gates based on the given condition. (C.O.No.1) [Knowledge Level]
23. NAND gate is used mostly for sum of product circuit implementation. The canonical sum of product form of the function $y(A, B)=A+B$ is $\qquad$ . (C.O.No.1) [Knowledge Level]

## Part B [Thought Provoking Questions]

## Answer all the Questions. Each question carries SIX mark.

24. A table is used to represent the Boolean expression of a logic gates function is called the logic gates. A logic gates truth table shows each possible input combination to the circuit with the resultant output depending upon the combination of the inputs.
(e) Find the Boolean expression in the standard sum of product (SOP) from the given truth table.
(f) Simplify the expression and implement (draw) using logic gates.

| Inputs |  |  | Outputs |
| :---: | :---: | :---: | :---: |
| $X$ | $Y$ | $Z$ | $F$ |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

$(2+2+2=6)$
(C.O. No-1) [Application Level]
25. In a certain chemical-processing plant, a liquid chemical is used in a manufacturing process. The chemical is stored in three different tanks. A level sensor in each tank produces a HIGH voltage when the level of chemical in the tank drops below a specified point.
Design and implement a circuit using AND-OR-NOT (AOI) logic that monitors the chemical level in each tank and indicates the level in any two of the tanks drops below the specific point.
(C.O. No-1, 2) [Application Level]
26. The digital system designer has a task to design the digital circuit. The circuit given below is the part of the very large digital circuit system. Use the given circuit and find the output expression of the given circuit.
(3+3=6 M) (C.O. No-1, 2) [Application Level]
(b)

(a)
(b)

(b)

## Part C [Problem Solving Questions]

Answer all the Questions. Each question carries TEN marks.
(2Qx10M=20M)
27. A combinational circuit is a type of a digital logic which is implemented by the Boolean expression circuits where the output is a pure function of a present inputs only. Half adder is such a combinational circuit which add two one-bit binary number.
(c) Draw the truth table of the half adder and implement the same using XOR and basic gates.
(d) Design and the full adder logic circuit using half adder circuits.
(11 marks) (C.O.No-2)[Application Level]
28. The K-Map (Karnaugh Map) is a method of simplifying Boolean expression. Maurice Karnaugh introduces this method in year 1953. K-Map can take two forms Sum of products (SOP) and Product of Sum (POS) according to the need of the problem. Don't care denotes inputs that are invalid for a given digital circuit. Thus, they can used to further simplify the Boolean output expression of a digital circuit. Don't care also prevents hazards in digital systems.
(d) Using the concept of the K-Map and don't care minimise the below given Boolean function in SOP minimal from using K-Map.

$$
F(A, B, C, D)=\sum m(1,2,6,7,8,13,14,15)+d(0,3,5,12)
$$

(e) Implement (draw) the simplified form using logic gates and tell the number of one input or two inputs logic gates required to implement.
(f) Comment why there is a need of minimisation in Boolean expression.

