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PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING
TEST 1

Winter Semester: 2021-22

Course Code:ECE 215

Course Name: VLSI DESIGN

Program &Sem:

Instructions:

(i) Read the all questions carefully and answer accordingly.

(ii) Non-Programmable Scientific Calculators permitted

Part A [Memory Recall Questions]

Answer all the Questions. Each question carries ONE mark. (10Qx 01M=10M)

1. Verilog has extensive logical operators. These operators perform logical operations such as AND,OR and XOR. For example, if A is the 4-bit signal 1011 and B is the 4-bit signal 1010, then find Z=~(A^B). (C.O.No.1) [KNOWLEDGE LEVEL]

2. Verilog arithmetic operators operate on numeric and array types. If operand B =10110,find the Z={3{B}}.
(C.O.No.1) [KNOWLEDGE LEVEL]

3. Several styles of code writing can be used to describe the system. Selection of the styles depends on the available information on the system. The _____description implements sequential execution of statements.
(C.O.No.1) [KNOWLEDGE LEVEL]

4. Verilog has the basic shift operators. Shift operators are unary operators, they operate on a single operand. If operand A is the four-bit vector 1111000 determine the A>>3 operation
(C.O.No.1) [KNOWLEDGE LEVEL]

5. A behavioral description models the system as to how the outputs behave with the inputs; usually, a flowchart is used to show this behavior. List 3 the conditional statements in Behavioral Description.
(C.O.No.1) [KNOWLEDGE LEVEL]
6. Arithmetic operators can perform a wide variety of operations, such as addition, subtraction, multiplication, and division. Verilog arithmetic operator which performs modulus.
(C.O.No.1) [KNOWLEDGE LEVEL]

7. Y chart helps to understand the processes overview in VLSI in a better way. It can be considered as a three axis based chart where all layers are interconnected. What should be the next procedure in Y chart after leaf cell?
(C.O.No.1) [KNOWLEDGE LEVEL]

8. Verilog supports several data types including nets, registers, vectors, integer, real, parameters, and arrays. Nets are declared by the predefined word_____.
(C.O.No.1) [KNOWLEDGE LEVEL]

9. Vectors are multiple bits. A register or a net can be declared as a vector. Vectors are declared by _____.
(C.O.No.1) [KNOWLEDGE LEVEL]

10. Any VLSI design block cannot be placed anywhere except the sequence which is given in the flow, as it depends on the abstraction levels as well. Considering the abstraction levels as per the sequence, Which is the next abstraction level after circuit?
(C.O.No.1) [KNOWLEDGE LEVEL]

Part B [Thought Provoking Questions]

Answer any ONE Question. Question carries TEN marks. (1Qx10M=0M)

11. Y chart helps to understand the process overview in VLSI in a better way. It can be considered as a three axis based chart where all layers are interconnected. As a student of VLSI Design of this semester illustrate Y chart as simplified design flow for IC design.
(C.O.No.1) [COMPREHENSIVE LEVEL]

12. There are a large number and variety of basic fabrication steps used in the production of modern MOS ICs. The same process can be used for the design of NMOS or PMOS or CMOS devices. The process may be viewed as a set of patterned layers of doped silicon, polysilicon, metal and insulating silicon dioxide, since each processing step requires that certain areas are defined on chip by appropriate masks. As a student of VLSI Design of this semester explain PMOS Fabrication steps with neat diagrams.
(C.O.No.2) [COMPREHENSIVE LEVEL]

Part C [Problem Solving Questions]

Answer both the Questions. Each question carries FIVE marks. (2Qx5M=10M)

13. Address decoding refers to the way a computer system decodes the addresses on the address bus to select memory locations in one or more memory or peripheral devices. Write a Verilog Code in Behavioral Description that has 3 address line and 8 data lines using Case statements. (C.O.No.1) [COMPREHENSIVE LEVEL]

14. Sixth semester students Abhinav has designee an 8 bit ALU using Verilog code. The opcode specifies the type of operation performed on register A and B. When he runs the code he gets an error “operand length mismatch”.
    i. Determine the line number in the code were he gets this error.
    ii. Type of Description followed in the given code
    iii. In Line 6 ‘ * ’ refers to?
    iv. Define register datatype.
    v. Number of operation can be increased if we increase the vector size of _____input. (C.O.No.1) [COMPREHENSIVE LEVEL]

15. **Line1:** **module** alu(A,B,Opcode, ALU_Out);
16. **Line2:input** [**7**:**0**] **A**,**B**; // ALU 8-bit Inputs
17. **Line3:input** [**1**:**0**] opcode;// ALU Selection
18. **Line4:output** [**7**:**0**] ALU_Out; // ALU 8-bit Output
19. **Line5: reg** [**7**:**0**] ALU_out;
20. **Line6:always** @(*)
21. **Line7:begin**
22. **Line8:case**(opcode)
23. **Line9:2'b00**: ALU_out =**A**+**B** ; // Addition
24. **Line10:2'b01**: ALU_out =**A**-**B** ; // Subtraction
25. **Line11:2'b10**: ALU_out =**A***B; // Multiplication
26. **Line12:Default:**ALU_out = {**A**,**B}**;// Concatenation
27. **Line13:endcase**
28. **Line14:end**
29. **Line15:endmodule**

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GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OFENGINEERING

TEST 2

Winter Semester: 2021-22
Course Code: ECE 215
Course Name: VLSI DESIGN
Program &Sem: B.Tech (ECE)&VI sem

Date : 1st June 2022
Time : 10:00 AM to 11:00 AM
Max Marks: 30M
Weightage :15%

Instructions:

(iii) Read the all questions carefully and answer accordingly.
(iv) Non-Programmable Scientific Calculators permitted

Part A[Memory Recall Questions]

Answer both the Questions. Each question carries FOUR marks. (2Qx 4M=8M)

1) Device scaling is an important part of the very large scale integration (VLSI) design to boost up the success path of VLSI industry, which results in denser and faster integration of the devices. In a constant electric field model, what is the scaling factor for Maximum Operating Frequency fo=$\frac{W}{L}\frac{\mu\, Co\, Vdd}{Cg}$ and Saturation Current Ids=$\frac{Co\mu\, W}{2L} * (Vgs - Vt)^2$?

(C.O.No.2) [KNOWLEDGE LEVEL]

2) The design of high-density chips in MOS VLSI (Very Large Scale Integration) technology requires that the packing density of MOSFETs used in the circuits is as high as possible and, consequently, that the sizes of the transistors are as small as possible. The reduction of the size, i.e., the dimensions of MOSFETs, is commonly referred to as scaling. Determine the scaling factor for Current Density J=$\frac{\mathrm{Ids}}{\mathrm{A}}$ and Channel Resistance Ron= $\frac{\mathrm{L}}{\mathrm{W}} * \frac{1}{\mathrm{Qon}*\mu}$ in general scaling model? (C.O.No.2) [KNOWLEDGE LEVEL]

Part B [Thought Provoking Questions]

Answer the following Question. The Question carries TEN marks. (1Qx10M=10M)

3) MOS transistor works by varying the width of a channel along which charge carriers flow (electrons or holes). The charge carriers enter the channel at source and exit via the drain. The voltage provided at the gate and drain ends controls the progressive change in channel width, which impacts current flow. As student of 6th semester derive the drain current expressions that relates to the gate-to-source and drain-to-source voltages for n channel MOSFET using Gradual

Channel Approximation. Plot the corresponding curves for the derived formula. [10M] (C.O.No.2) [COMPREHENSIVE LEVEL]

Part C [Problem Solving Questions]

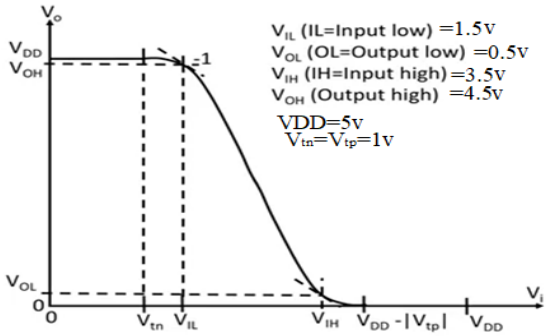
Answer all the Questions. Each question carries FOUR marks. (3Qx4M=12M)

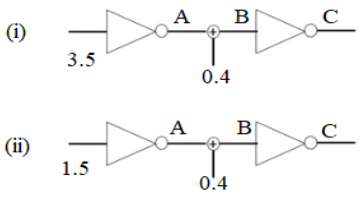
4). For an NMOS transistor, with following parameters:

i) Substrate doping density $N_A = 10^{16}$ cm^{-3}
ii) Polysilicon gate doping density $N_D = 2X10^{20}$ cm^{-3}
iii) Gate oxide thickness t_{ox}=500 Å
iv) Oxide interface fixed charge density $N_{ox} = 4X10^{10}$ cm^{-2}
v) Fermi potential of polysilicon gate=0.55V
vi) Intrinsic concentration $n_i = 1.45X10^{10}$ cm^{-3}
vii) KT/q=0.026
viii) V_{SB}=0V
ix) $q = 1.6X10^{-19}$ C
x) permittivity of free spaceϵ_0=8.85X10-14, permittivity of si $\epsilon_{si}=11.7\epsilon_0$, permittivity of oxide$\epsilon_{ox}=3.97\epsilon_0$.
Calculate Fermi potential, work function difference between gate and channel, gate oxide capacitance per unit area, threshold voltage?

[4M] (C.O.No.2) [COMPREHENSIVE LEVEL]

5). Noise margin is the amount of noise that a CMOS circuit could withstand without compromising the operation of circuit. Noise margin does makes sure that any signal which is logic '1' with finite noise added to it, is still recognized as logic '1' and not logic '0'. List the formulas for Noise Margin Low and Noise Margin High. Determine the output for the given circuit (at points A, B and C) using the VTC CMOS Inverter Characteristics.





[4M] (C.O.No.3) [COMPREHENSIVE LEVEL]

6) For an NMOS transistor, with following parameters:
L=2µm, W=10µm, µn=0.06 m^2/Vs , Cox=$1.5x10^{-4}$F/m2 V_{to}=0.4,V_{gs}=0.9V
Determine Drain current I_{ds} when (i)V_{ds} =0.2 V and (ii)V_{ds}=0.7V.

[4M](C.O.No.2) [COMPREHENSIVE LEVEL]

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BENGALURU
SCHOOL OF ENGINEERING

END TERM EXAMINATION

Winter Semester: 2021-22

Course Code: ECE215

Course Name: VLSI DESIGN

Program &Sem:

Instructions:

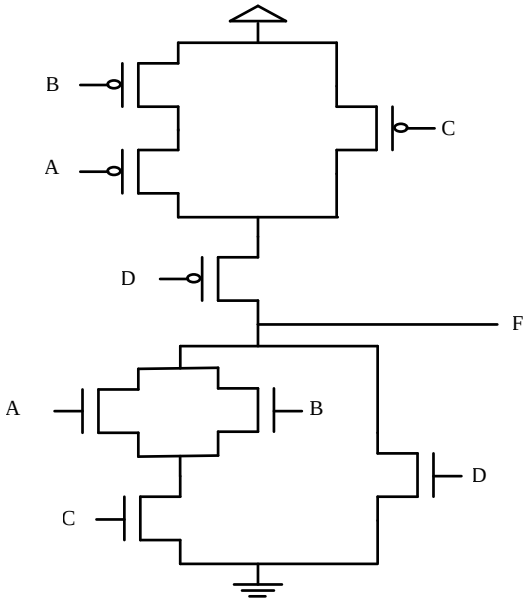
(v) Read the all questions carefully and answer accordingly.

(vi) Non-Programmable Scientific Calculators permitted

Part A[Memory Recall Questions]

Answer all the Questions. Each question carries FOUR marks. (10Qx 4M=40M)

1. CMOS logic design is commonly used logic style for designing digital circuits. Here, the circuit consists of both pull up network and pull down network consisting of PMOS & NMOS transistors respectively. Determine the Boolean function for the CMOS circuit illustrated in the diagram below:



(C.O.No.3) [KNOWLEDGE LEVEL]

2. Verilog is a Hardware Description Language; a textual format for describing electronic circuits and systems Write a Verilog code for NAND gate using Data flow Description.

(C.O.No.1)

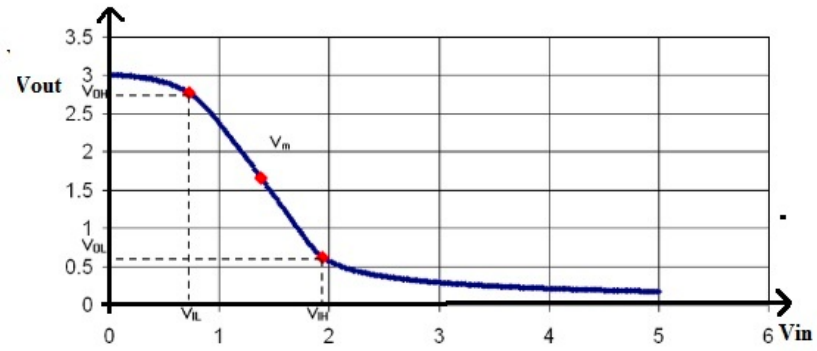
[KNOWLEDGE LEVEL]

3. The design flow of VLSI system takes into account the various representations, or abstractions of design: behavioral, logic , circuit and mask layout. Draw the design flow chart for VLSI design. (C.O.No.1) [KNOWLEDGE LEVEL]
4. The Y chart aids in the better understanding of the VLSI process overview. It's a three-axis graph with interconnected layers. Draw the Y chart for VLSI design. (C.O.No.1) [KNOWLEDGE LEVEL]
5. Lambda (λ)-based design rules, all paths in all layers will be dimensioned in λ units and subsequently. λ can be allocated an appropriate value compatible with the feature size of the fabrication process. Using Lambda based design rules draw the transistor representation. (C.O.No.3) [KNOWLEDGE LEVEL]
6. The design of high-density chips in MOS VLSI (Very Large Scale Integration) technology requires that the packing density of MOSFETs used in the circuits is as high as possible and, consequently, that the sizes of the transistors are as small as possible. The reduction of the size, i.e., the dimensions of MOSFETs, is commonly referred to as scaling. Determine the scaling factor Channel Resistance Ron= $\frac{\mathrm{L}}{\mathrm{W}} * \frac{1}{\mathrm{Qon}*\mu}$ and Ids=$\frac{Co\mu\, W}{2L} * (Vgs - Vt)^2$in general scaling model? (C.O.No.2) [KNOWLEDGE LEVEL]
7. A Full Adder's circuit can be used as a part of many other larger circuits like Ripple Carry Adder, which adds n-bits simultaneously. Write a Verilog Code for full adder in Structural Description. (C.O.No.3) [KNOWLEDGE LEVEL]
8. A multiplexer (MUX) is a combinational circuit that uses several data inputs to generate a single output. Write a Verilog Code for 4:1 MUX using behavioral description. (C.O.No.1) [KNOWLEDGE LEVEL]
9. Today, CMOS technology is the dominant IC fabrication technology in VLSI industry and is used for making high end microprocessors, microcontroller, memory modules, sensors and Application Specific Integrated Circuits (ASICs). Use CMOS technology to implement an OR gate. (C.O.No.3) [KNOWLEDGE LEVEL]
10. The design of high-density chips in MOS VLSI (Very Large Scale Integration) technology requires that the packing density of MOSFETs used in the circuits is as high as possible and, consequently, that the sizes of the transistors are as small as possible. The reduction of the size, i.e., the dimensions of MOSFETs, is commonly referred to as scaling. List different scaling models in VLSI. (C.O.No.3) [KNOWLEDGE LEVEL]

Part B [Thought Provoking Questions]

Answer all the Questions. Each question carries TEN marks. (3Qx10M=30M)

11. The quality of the inverter can be measured frequently by using the VTC or voltage transfer curve, which is plotted between input voltage (Vin) and output voltage (Vo). From the following static characteristics of CMOS inverter, depict following parameter:
    I. identify Five region of operation in the graph.
    II. Identify the PMOS and NMOS transistor mode of operation in each region.
    III. Switching threshold operates in _____ region .
    IV. Regions were Gain is -1
    V. Establish a noise margin From VTC, calculate the NML and NMH equations.



Voltage Transfer Curve

(C.O.No.3) [COMPREHENSIVE LEVEL]

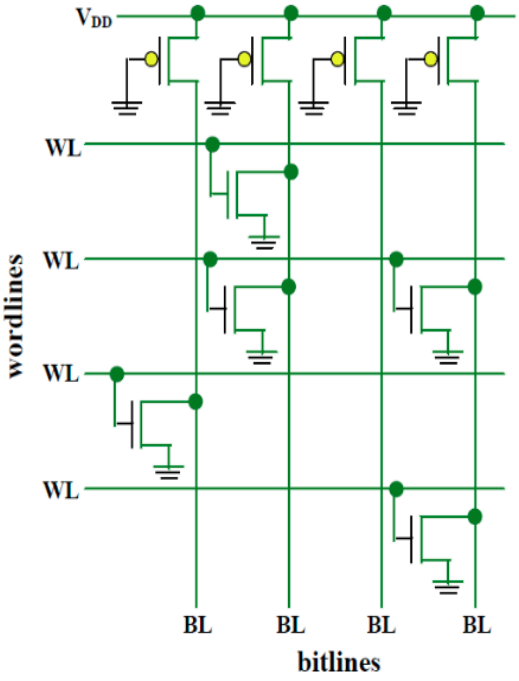
12. Cache memory is a chip-based computer component that makes retrieving data from the computer's memory more efficient. It acts as a temporary storage area that the computer's processor can retrieve data from easily. What RAM is used to create cache memories, and why? Draw a simple DRAM diagram and describe the read and write processes. (C.O.No.3) [COMPREHENSIVE LEVEL]
13. In VLSI design, as processes become more and more complex, need for the designer to understand the intricacies of the fabrication process and interpret the relations between the different photo masks is really troublesome. Therefore, a set of layout rules, also called design rules, has been defined. They act as an interface or communication link between the circuit designer and the process engineer during the manufacturing phase. As student of 6th semester explain design rules for WELL.
(C.O.No.3) [COMPREHENSIVE LEVEL]

Part C [Problem Solving Questions]

Answer all the Questions. Each question carries TEN marks.
(3Qx10M=30M)

14.

a) A NOR-based ROM consists of m n-input pseudo-nMOS NOR gates, one n-input NOR per column as shown in Figure . Each memory cell is represented by one nMOS transistor and a binary information is stored by connecting or not the drain terminal of such a transistor to the bit line. Determine the binary data stored in each row.



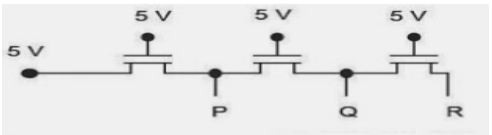
b) A NAND-based ROM consists of depletion load NAND driven by row signals(word line). Design 4x4 NAND based ROM that stores binary information at a particular address location as shown below.

R1	R2	R3	R4	C1	C2	C3	C4
0	1	1	1	0	1	0	1
1	0	1	1	0	0	1	1
1	1	0	1	1	0	0	1
1	1	1	0	0	1	1	0

(C.O.3)[Comprehension level]

15.

a) In the following circuit employing pass transistor logic ,all NMOS transistors are identical with threshold voltage of 0.5 V Ignoring the body effect, find the voltage P ,Q,R?



b) Implement the following boolean expression using NMOS technology and Draw the corresponding stick diagram

$$f = [(xy) + z]'$$

(C.O.3)[Comprehension level]

16.

Today, CMOS technology is the dominant IC fabrication technology in VLSI industry and is used for making high end microprocessors, microcontroller, memory modules, sensors and Application Specific Integrated Circuits (ASICs)..

a) Implement the following boolean expression using CMOS technology $f = \big((a+b)c\big)'$
b) Draw the corresponding stick diagram(use Eulers Rule)

(C.O.3)[Comprehension level]