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GAIN MORE KNOWLEDGE
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PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

TEST 1

Winter Semester: 2021 - 22

Course Code: ECE 323

Course Name: VLSI CAD TOOLS

Program & Sem: B.Tech & VI Semester

Date: 26th April 2022

Time: 1:30 PM to 2:30 PM

Max Marks: 30

Weightage: 15%

Instructions:

(i) Read the all questions carefully and answer accordingly.
(ii) Use of Scientific (non-programmable) calculators are permitted.

Part A [Memory Recall Questions]

Answer all the Questions. Each question carries ONE mark. **(8Qx 1M= 8M)**

1. Computational complexity refers to the time and memory required by a certain algorithm, the complexity will depend on which algorithm's function?

a) Size of the algorithm's output
b) Size of the algorithm's input
c) Both a & b
d) None of the above

(C.O.No.1) [Knowledge]

2. Which among the following is a process of transforming design entry information of the circuit into a set of logic equations?

a) Simulation
b) Optimization
c) Synthesis
d) Verification

(C.O.No.1) [Knowledge]

3. Which among the following is/are regarded as the function/s of translation step in synthesis process?

a) Conversion of RTL description to Boolean un-optimized description
b) Conversion of an un-optimized to optimized Boolean description
c) Conversion of un-optimized Boolean description to PLA format
d) All of the above

(C.O.No.1) [Knowledge]

4. A single interchange format is introduced to avoid all the problems involved in interchanging data from one tool to other, so that all tools could read and write. A famous interchange format is EDIF, which stands for? (C.O.No.1) [Knowledge]

a) Electronic Device Interchange Format
b) Electronic Design Interchange Format
c) Electronic Design Interconnection Format
d) None of the above

5. Graph is a mathematical structure that describes a set of objects and the connections. A graph is characterized by two sets namely?

a) Vertex set V
b) Edge set E
c) Both of the above
d) None of the above

(C.O.No.1) [Knowledge]

6. Building the system to be designed from discrete components rather than one or a few integrated circuits is called as?

a) Prototyping
b) Simulation
c) Formal Verification
d) None of the above

(C.O.No.1) [Knowledge]

7. When one removes vertices and/or edges from a given graph G, one gets a subgraph of G. In this process, the one or more vertices will be removed from a graph. Removing a vertex implies?

a) Removal of all edges connected to it.
b) Removal of any one edge connected to it.
c) Removal of vertices adjacent to it.
d) None of the above.

(C.O.No.1) [Knowledge]

8. If the vertex set V of a graph is the union of two disjoint sets V1 and V2 and all edges of this graph exclusively connect a vertex from V1 with a vertex V2, the graph is called?

a) Connected.
b) Directed.
c) Bipartite.
d) None of the above.

(C.O.No.1) [Knowledge]

Part B [Thought Provoking Questions]

Answer both the Questions. Each question carries SIX marks. (2Qx6M=12M)

9. The VLSI circuits designed can be categorized as general-purpose integrated circuits and application-specific integrated circuits (ASICs). General-purpose integrated circuits are characterized by a wide range of applications such as microprocessors, digital signal processors, and memories. Application-specific integrated circuits (ASICs) are designed for a narrow range of applications (or even a single one). Designing a circuit such as ASIC is a difficult task, there are different entities that one has to optimize by maintaining the tradeoff between all required entities. Identify the different entities which can be optimized by VLSI design Engineer?

(C.O.No.1) [Comprehension]

10. a) Designing an integrated circuit is a sequence of many actions most of which can be done by computer tools. The designer is mainly concerned with the initial algorithm to be implemented in hardware and works with a purely behavioral description of it. Describe about the Algorithmic and System Design and locate the tools on Y-Chart?

b) Logic synthesis is concerned with the generation and optimization of a circuit at the level of Boolean gates. Identify and describe the three different types of logic synthesis problems?

(C.O.No.1) [Comprehension]

Part C [Problem Solving Questions]

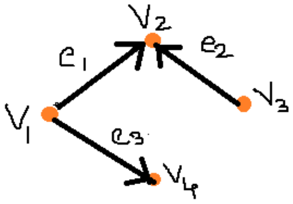
Answer the following Question. The question carries TEN marks. (1Qx10M=10M)

11. An algorithm operates on edges rather than on vertices and needs to efficiently identify the vertices that an edge connects, a data structure that is built from explicit structures, can be used for both vertices and edges. Algorithmic Graph is used to represent behavior of any complex circuit. Any algorithmic graph can be represented in C language using data structure. Adjacency matrix and adjacency list are the methods to represent the relation between vertices and edges and how they are connected. For given graph below:

a) Find the adjacency matrix?

b) Draw the adjacency list?

b) Visualizing the edge and vertex structures built from data structures represent the given graph?



(C.O.No.1) [Analysis]

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SCHOOL OF ENGINEERING

TEST – 2

Winter Semester: 2021 - 22

Course Code: ECE 323

Course Name: VLSI CAD Tools

Program & Sem: B. Tech., 6th Semester

Date: 1st June 2022

Time: 01:30 PM to 02:30 PM

Max Marks: 30

Weightage: 15 %

Instructions:

(i) Read the all questions carefully and answer accordingly.

(ii) Use of scientific (non – programmable) calculators is permitted

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Part A [Memory Recall Questions]

Answer all the Questions. Each question carries TWO marks. (3Qx 2M= 6M)

Q.NO 1. The problems in the optimization of combinational circuit are referred as Decision problem. Depict the classification of all decision problems in circuit design. (C.O.No.2) [Knowledge]

Q.NO 2. Layout is the representation of CMOS circuits for real time implementation. Define layout compaction? (C.O.No.3) [Knowledge]

Q.NO 3. In VLSI design flow, the physical design steps are the core of IC fabrication. In physical design, the placement is the process of finding a suitable physical location for each cell in the block. To accomplish the optimized placement, describe the goals of Placement? (C.O.No.3) [Knowledge]

Part B [Thought Provoking Questions]

Answer both the Questions. Each question carries SIX marks. (2Qx6M=10M)

Q.NO 4. Placement is integral part of the physical design of the VLSI Design flow**.** There are two types of Placement algorithms in real time. Differentiate between the Iterative Placement and Constructive Placement with examples (C.O.No.3) [Analyze]

Q.NO 5. The layout is the physical realization of circuits that consists of CMOS transistors. The layout follows certain rules in the design of circuits. Making use of the design rules, depict the CMOS inverter stick diagram with the CMOS circuit diagram. (C.O.No.3) [Application]

Part C [Problem Solving Questions]

Answer the Question. The question carries TWELV marks. (1Qx12M=12M)

Q.NO 6. In VLSI, the circuit design needs to be translated into a model to provide upgradability in the IC design process. The representation of the circuit depends on the design demand of the application. The cell-port-net data model is used to represent any given circuit. Now, derive the Clique model for the RS-Latch as depicted in Fig.1

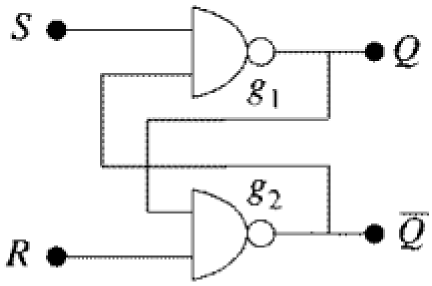

Fig.1

[12 Marks] (C.O.No.3) [Application]

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END TERM EXAMINATION

Winter Semester: 2021 - 22
Course Code: ECE 323
Course Name: VLSI CAD Tools
Program & Sem: B. Tech., 6th Semester/PhD

Date: 30th June 2022
Time: 9:30 AM to 12:30 PM
Max Marks: 100
Weightage: 50 %

Instructions:

(i) Read the all questions carefully and answer accordingly.
(ii) Use of scientific (non – programmable) calculators is permitted

Part A [Memory Recall Questions]

Answer all the Questions. Each question carries TWO marks. **(10Q x 2M = 20M)**

Q.NO 1. In VLSI design, the design methodology is classified into several types. Differentiate between Full Custom IC and Semi-Custom IC

(C.O.No.1) [Knowledge]

Q.NO 2. The complex computational problems in design can be resolved in algorithmic graph theory. Distinguish between the Polynomial Time and Non-deterministic Polynomial Time

(C.O.No.2) [Knowledge]

Q.NO 3. A stick diagram representation is intermediate to the circuit design and layout. Depict the stick diagram of an Inverter.

(C.O.No.2) [Knowledge]

Q.NO 4. The algorithmic graph theory is utilized for the complex computation problems. Define complete graph with example

(C.O.No.1) [Knowledge]

Q.NO 5. The logic circuits are represented using the graph model for reducing the complexity. Draw the Clique model of the RS Flip Flop.

(C.O.No.1) [Knowledge]

Q.NO 6. The VLSI design flow involves several steps in the design of Integrated circuit. In VLSI design flow, highlight the importance of design rule check.

(C.O.No.4) [Knowledge]

Q.NO 7. In VLSI design, the circuit designs are represented using the mathematical models. Define Formal verification and explain the disadvantages.

(C.O.No.2) [Knowledge]

Q.NO 8. In Standard cell IC, the terminals are provided in horizontal and vertical direction. Distinguish between the logic signals and logistic signals?

(C.O.No.3) [Comprehension]

Q.NO 9. The issues in routing can be eradicated by using constraint graph algorithms. Explain the doglegging in channel routing.

(C.O.No.4) [Comprehension]

Q.NO 10. Routing is the process used for the connection of placed block in the VLSI design. Differentiate between the Global Routing and Local Routing

(C.O.No.4) [Comprehension]

Part B [Thought Provoking Questions]

Answer all the Questions. Each question carries EIGHT marks. (4Q x 8M = 32M)

Q.NO 11. The placement is achieved by two methodologies namely heuristic and iterative algorithms. Iterative uses the high level compilers to optimize the placement of blocks in IC design. Develop the code for the iterative Placement with suitable examples

(C.O.No.3) [Application]

Q.NO 12. The CMOS circuits is used to realize the IC design in Real time based on the layout rules. Identify the layout rules applicable for the development of CMOS based circuit design.

(C.O.No.3) [Application]

Q.NO 13. Though the Vertical and Horizontal Constraint Graph are used to address the issues in the routing of terminals, the left-edge algorithm is used for channel routing. Construct the Left-edge algorithm for Channel routing with suitable example.

(C.O.No.4) [Application]

Q.NO 14. The size of the blocks that are used in the floorplan are to be optimized with respective to the available area in the IC design. Illustrate the optimization of floorplan sizing for two cells C1 and C2 with 4X2 and 5X3 sizes respectively.

(C.O.No.3) [Application]

Part C [Problem Solving Questions]

Answer all the Questions. Each question carries TWELVE marks. (4Q x 12M = 48M)

Q.NO 15. The placement process is highly important in the design of ICs. The Mincut algorithm is suitable for placements. Develop the optimized partition for the following diagram using the Kernighan-Lin Algorithm

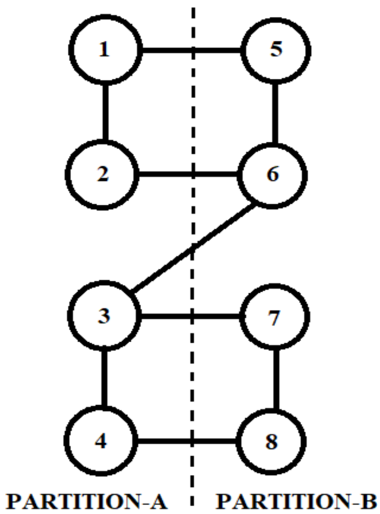

Fig.1

(C.O.No. 3) [Application]

Q.NO 16. The layout is the physical realization of circuits that consists of CMOS transistors. The layout follows certain rules in the design of circuits. Making use of the design rules, depict the CMOS NOR stick diagram along with the CMOS circuit diagram.

(C.O.No. 2) [Application]

Q.NO 17. The source and terminals nodes are to be interconnected using the routing methods as shown in Fig.2. Utilize the Maze Routing Algorithm to interconnect the terminals with necessary diagrams.

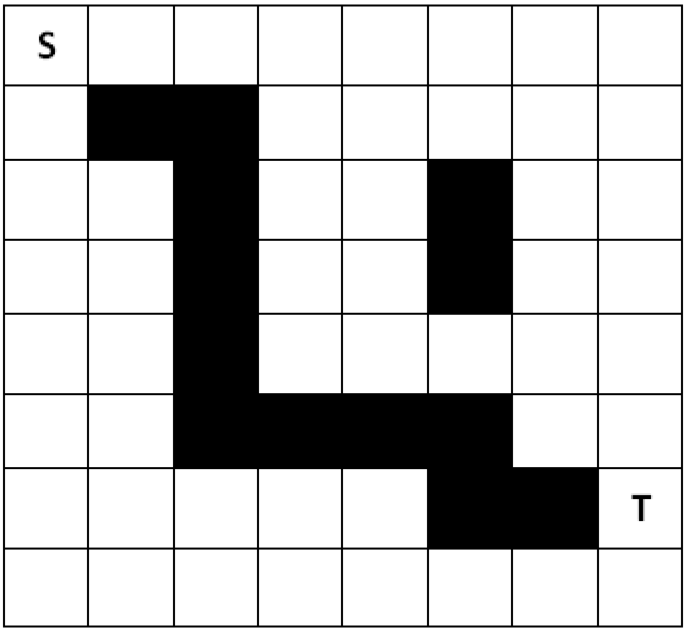

Fig. 2

(C.O.No. 4) [Application]

Q.NO 18. The complex computations are resolved using the Algorithmic Graph theory representation of digital design without including specific hardware. Develop the Depth First search algorithm using necessary example.

(C.O.No. 1) [Application]