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PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING
END TERM EXAMINATION - JAN 2023

Semester : Semester III - 2021
Course Code : EEE2015
Course Name : Sem III - EEE2015 - Digital Electronics
Program : B.Tech. Electrical and Electronics Engineering

Date : 16-JAN-2023
Time : 1.00PM - 4.00PM
Max Marks : 100
Weightage : 50%

Instructions:
(i) Read all questions carefully and answer accordingly.
(ii) Question paper consists of 3 parts.
(iii) Scientific and non-programmable calculator are permitted.

PART A

ANSWER ALL THE TEN QUESTIONS **10 X 2 = 20M**

1. Variable, complement, and literal are terms used in Boolean algebra. In Boolean algebra, a sum term is a sum of literals. The Boolean expression $A + B + C$ is

a) a sum term (CO1) [Knowledge]
b) a literal term
c) an inverse term
d) a product term

2. Converting a binary number to hexadecimal is a straightforward procedure. Simply break the binary number into 4-bit groups. The binary number 10001101010001101111 can be written in hexadecimal as

a) AD467 (CO1) [Knowledge]
b) 8C46F
c) 8D46F
d) AE46F

3. A simplified Boolean expression uses the fewest gates possible to implement a given expression .To implement the expression , it takes

a) five AND gates, one OR gate, and eight inverters (CO2) [Knowledge]
b) four AND gates, two OR gates, and six inverters
c) five AND gates, three OR gates, and seven inverter
d) five AND gates, one OR gate, and seven inverters

4. A form of Boolean expression that is basically the ANDing of ORed terms. The Boolean expression X = (A + B)(C + D) represents

a) two ORs ANDed together (CO2) [Knowledge]

b) two ANDs ORed together

c) A 4-input AND gate

d) a 4-input OR gate

5. A digital circuit that adds two bits and produces a sum and an output carry. It cannot handle input carries.A half-adder is characterized by

a) two inputs and two outputs (CO3) [Knowledge]

b) three inputs and two outputs

c) two inputs and three outputs

d) two inputs and one output

6. Two or more full-adders are connected to form parallel binary adders. A 3-bit parallel adder can add

a) three 2-bit binary numbers (CO3) [Knowledge]

b) two 3-bit binary numbers

c) three bits at a time

d) three bits in sequence

7. When the input bits are both 1 and the input carry bit is 1, the sum output of a full adder is 1.. A full-adder is characterized by

a) two inputs and two outputs (CO3) [Knowledge]

b) three inputs and two outputs

c) two inputs and three outputs

d) two inputs and one output

8. A flip-flop changes its state during the

a) complete operational cycle (CO4) [Knowledge]

b) falling edge of the clock pulse

c) rising edge of the clock pulse

d) both answers (b) and (c)

9. A Moore state machine consists of combinational logic circuits that determine

a) sequences (CO4) [Knowledge]

b) memory

c) both (a) and (b)

d) neither (a) nor (b)

10. J-K flip-flop A type of flip-flop that can operate in the SET, RESET, no-change, and toggle modes. A feature that distinguishes the J-K flip-flop from the D flip-flop is the

a) toggle condition (CO4) [Knowledge]

b) preset input

c) type of clock

d) clear input

PART B

ANSWER ALL THE FOUR QUESTIONS **4 X 10 = 40M**

11. Each product term in an SOP expression that does not contain all the variables in the domain can be expanded to standard form to include all variables in the domain and their complements. Convert the following Boolean expression into standard SOP form: AB'C + A' B' + ABC'D.

(CO1) [Comprehension]

12. Karnaugh map An arrangement of cells representing the combinations of literals in a Boolean expression and used for a systematic simplification of the expression. Use a Karnaugh map to simplify each expression to a minimum SOP form:

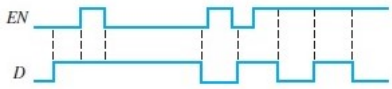
(a) $\overline{A}B\overline{C} + A\overline{B}C + \overline{A}BC + AB\overline{C}$ (b) $AC[\overline{B} + B(B + \overline{C})]$

(CO2) [Comprehension]

13. The basic function of a comparator is to compare the magnitudes of two binary quantities to determine the relationship of those quantities. Design a 2-bit comparator and implement it using logic groups.

(CO3) [Comprehension]

14. For a gated D latch, the waveforms shown in Figure below are observed on its inputs. Draw the timing diagram showing the output waveform you would expect to see at Q if the latch is initially RESET.

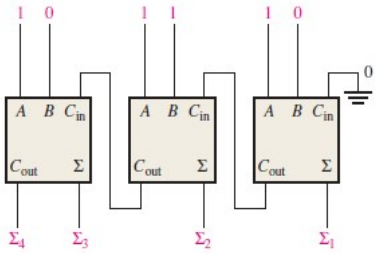


(CO4) [Comprehension]

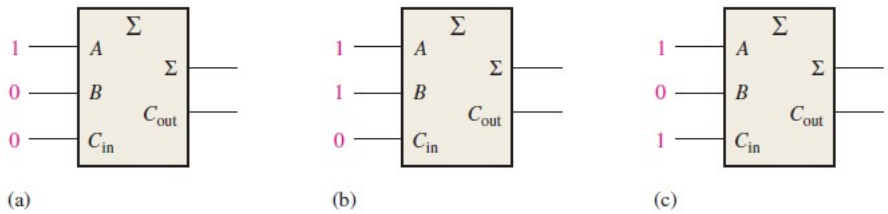
PART C

ANSWER ALL THE TWO QUESTIONS **2 X 20 = 40M**

15. a. Two or more full-adders are connected to form parallel binary adders. For the parallel adder in Figure, compute the complete sum by analysis of the logical operation of the circuit.



b. For each of the three full-adders in Figure, compute the outputs for the inputs shown.



(CO3) [Application]

16. a. The application of a flip-flop is dividing (reducing) the frequency of a periodic waveform.Develop the fout waveform by showing a flip flop arrangement, when an 8 kHz square wave input is applied as shown in below figure to the clock input of flip-flop A.

b. The serial in/serial out shift register accepts data serially—that is, one bit at a time on a single line. It produces the stored information on its output also in serial form. Show the Shifting of a 4-bit code of 1111 into the shift register.

(CO4) [Application]

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