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PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING
END TERM EXAMINATION - JAN 2023

Semester : Semester III - 2021
Course Code : CSE2009
Course Name : Sem III - CSE2009 - Computer Organization and Architecture
Program : B.Tech. CSE (All)

Date : 18-JAN-2023
Time : 1.00PM - 4.00PM
Max Marks : 100
Weightage : 50%

Instructions:
(i) Read all questions carefully and answer accordingly.
(ii) Question paper consists of 3 parts.
(iii) Scientific and non-programmable calculator are permitted.

PART A

ANSWER ALL THE TEN QUESTIONS **10 X 2 = 20M**

1. List the different types of registers inside the processor of a Computer System.
(CO1) [Knowledge]

2. List out the methods used to improve system performance.
(CO1) [Knowledge]

3. What do you mean by Register transfer?
(CO1) [Knowledge]

4. List out the additional modes used by the processor.
(CO2) [Knowledge]

5. What is the advantage and disadvantage of direct mapping in cache memory?
(CO2) [Knowledge]

6. Distinguish write-through and write-back policies of updating cache.
(CO2) [Knowledge]

7. Give the generation and propagation functions used in Carry look ahead adder.
(CO3) [Knowledge]

8. Mention the group of lines in the system bus?
(CO3) [Knowledge]

9. Differentiate between multiple bus organization and single bus organization?
(CO4) [Knowledge]

10. What are the various stages in a pipeling execution.
(CO4) [Knowledge]

PART B

ANSWER ALL THE FIVE QUESTIONS **5 X 10 = 50M**

11. Discuss the factors that affect the performance of the computer. Let a processor operates by a frequency 10MHtz and it executes a typical program in which 50% are register referenced instruction,30% are memory reference instructions and 20% are branch instructions. Register referenced instruction , memory reference instructions and branch instructions take 4, 8 and 6 clock cycles respectively. then find out the total time taken by the processor to execute the program.

(CO1) [Comprehension]

12. Registers R1 and R2 of a computer contains the decimal value 1100 and 500.
What is the effective address of the memory operand in each of the following instruction?
i) Load 20(R1),R5
ii) Move 300,R5
iii) Store R5, 50(R1,R2)
iv) Subtract (Ri) +, R5
v) AND R1,R2

(CO2) [Comprehension]

13. Multiply each of the following pairs of signed 2's complement number using the Booths algorithm. (A=Multiplicand and B=Multiplier)
a) A=010111 and B=110110
b) A=110011 and B=101100

(CO3) [Comprehension]

14. Illustrate the steps involved in an DMA operation with Cycle Stealing and Burst Mode with proper diagram.

(CO3) [Comprehension]

15. With diagram, describe the internal organisation of a 128 X 8 memory chip. How many separate address and data lines are needed for the design.

(CO2) [Comprehension]

PART C

ANSWER ALL THE TWO QUESTIONS **2 X 15 = 30M**

16. Cache mapping is a technique that defines how contents of main memory are brought into cache memory. Expalin different cache mapping techniques with suitable examples.

(CO2) [Application]

17. The component of the processor that performs arithmetic operations are connected to a datapath. Illustrate the same with neat diagram for single datapath inside the processor. Write the control sequence for execution of the instruction "Add (R1), R2"

(CO4) [Application]

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