## PRESIDENCY UNIVERSITY

BENGALURU

## SCHOOL OF INFORMATION SCIENCE END TERM EXAMINATION - JAN 2023

Semester : Semester I-2022
Course Code : ECE2009
Course Name : Sem I-ECE2009 - Digital Computer Fundamentals
Program : BCA / BCG / BCV

Date: 9-JAN-2023
Time : 9.30AM - 12.30PM
Max Marks : 100
Weightage : 50\%

## Instructions:

(i) Read all questions carefully and answer accordingly.
(ii) Question paper consists of 3 parts.
(iii) Scientific and non-programmable calculator are permitted.

PART A
ANSWER ALL THE FOLLOWING QUESTIONS
$15 \times 2=30 \mathrm{M}$

1. A K-map of 3 variables contains $\qquad$ Cells.
a. 6
b. 3
c. 8
d. 9
(CO1) [Knowledge]
2. The basic operations of Boolean algebra are as follows: 1. Conjunction or AND operation 2. Disjunction or OR operation 3. Negation or Not operation. Below is the table definingthe symbols for all three basic operations. As per De-Morgans's Law for 3 Variables:
i) $(A+B+C)^{\prime}=$ $\qquad$ ?
ii) $(A . B . C)^{\prime}=$ $\qquad$ ?
(CO1) [Knowledge]
3. The basic operations of Boolean algebra are as follows: 1. Conjunction or AND operation 2. Disjunction or OR operation 3. Negation or Not operation. Below is the table defining the symbols for all three basic operations. As per Boolean Algebra's Law for 3 Variables:
i) $(A+A ' B)=$ $\qquad$
ii) $\left(A^{\prime}+A C\right)=$ $\qquad$ ?
iii) $\left(A+A^{\prime}\right)=$ $\qquad$ ?
4. Boolean Algebra is used to analyze and simplify the digital (logic) circuits. It uses only the binary numbers i.e. 0 and 1. It is also called as Binary Algebra or logical Algebra.
From Boolean Postulate i) $\mathrm{A}^{\prime}+\mathrm{A}^{\prime} \mathrm{B}=$ $\qquad$ ii) $A B+A=$ $\qquad$
(CO1) [Knowledge]
5. The demultiplexer is used as a serial to parallel conversion circuit in digital based system. Mention number of selection lines required for 1:3 and 1:6.
(CO2) [Knowledge]
6. If the number of select lines in a multiplexer is 5 , then identify the MUX.
a. $32 \times 1$
b. $16 \times 1$
c. $8 \times 1$
d. $64 \times 1$
(CO2) [Knowledge]
7. The decoder is used to design the chip select signal circuit. Write the truth table of $2: 4$ decoder.
(CO2) [Knowledge]
8. The multiplexer is used as a data selector in digital based system. Draw the schematic view of the $4: 1$ multiplexer.
(CO2) [Knowledge]
9. The multiplexer is a combinational logic circuit designed to switch one of several input lines to a single common output line. Choose the applications of a MUX from the following
a. It is used as a data selector from many inputs to get one output.
b. These are used in the data acquisition system.
c. Both a \& b
d. Neither a nor b
(CO2) [Knowledge]
10. An arithmetic circuit that adds two bits and produces a sum bit (s) and carry bit (c) both as output is
a. Half Adder
b. Full Adder
c. Both a \& b
d. Neither a nor b
(CO2) [Knowledge]
11. A flip-flop is a circuit that has two stable states and can be used to store state information. Select appropriately where do you think flip flops are used.
a. Flip-flops are used as the delay element.
b. Flip-Flops are used as the memory element.
c. Both a \& b
d. Neither a nor b
(CO3) [Knowledge]
12. In a SR Flip Flop, $J$ and $K$ inputs are set to Logic 1, then the output $Q$ \& $Q$ ' will be ....
a. 0,0
b. 1,1
c. INVALID STATE
d. 1,0
(CO3) [Knowledge]
13. If O's are applied simultaneously to both set and reset input lines of a NAND-SR Flip Flop, then the mode of operation will be. $\qquad$
a. Set State
b. Reset State
c. Invalis State
d. Hold / Memory State
(CO3) [Knowledge]
14. JK flip flop is designed to overcome the invalid state of SR flip flop. Illustrate hold and toggle state input, $\mathrm{J}=$ ? and $\mathrm{K}=$ ? respectively.
(CO3) [Knowledge]
15. If 1 is applied simultaneously to $T$ input of $a-T$ Flip Flop, then the mode of operation will be
a. Set State
b. Toggle State
c. Invalis State
d. Hold / Memory State
(CO3) [Knowledge]

## PART B

## ANSWER ALL THE FOLLOWING QUESTIONS <br> $3 \times 10=30 M$

16. a) NAND gate is universal gate to implement any digital logic. Draw the XNOR logic using only NAND gates.
b) Each term in canonical form contains all possible literals. Convert the Boolean expression $Y=A C^{\prime}+B^{\prime}+A+A B C$ into canonical form.
c) Implement the below Boolean Expressions using NAND-Gates ONLY: i) $Y=A+B+C+D$
ii) $F=A . B . C . D$
(CO1) [Comprehension]
17. The Demultiplexer refers to the type of combinational circuit that accepts just a single input but directs it through multiple outputs. Illustrate the Working of 1:2 and 1:4 DEMUX with relevant Block Representation, Truth-Table, Logical Expression and BASIC GATES Implementation.
(CO2) [Comprehension]
18. The major difference between flip-flop and latch is that the flip-flop is an edge-triggered type of memory circuit while the latch is a level-triggered type. It means that the output of a latch changes whenever the input changes. On the other hand, the latch only changes its state whenever the control signal goes from low to high and high to low. The flip flop is used for designing counter and shift register circuit. Illustrate the working of T Flip Flop using the Truth Table, Characteristics Table and Characteristics Equation. Justify name of the T-Flip-Flop.
(CO3) [Comprehension]

## PART C

## ANSWER ALL THE FOLLOWING QUESTIONS

$4 \times 10=40 \mathrm{M}$
19. A digital system is to be designed in which the month of the year is given as input is four-bit form. The month January is represented as '0000', February '0001' and so on. The output of the system should be ' 1 ' corresponding to the input of the month containing 31 days or otherwise it is ' 0 '. Consider the excess numbers in the input beyond '1011' as don't care conditions for system of four variables (A, B, C, D). Design a Combinational logic circuit based on given Scenario using NAND Gates.
(CO1) [Application]
20. The demultiplers and multiplexer examples of Combinational networks used for designing digital circuits. Design full adder circuit with relevant Truth-Table using
i) $4: 1$ Multiplexer (ii) $8: 1$ multiplexer.
(CO2) [Application]
21. A decoder is a device that generates the original signal as output from the coded input signal. Explain the $2 \times 4$ decoder with block diagram and implementation using basic gates.
(CO2) [Application]
22. Flip flops are edge triggered one bit memory devices. They are used for designing counter and shift register circuit. Illustrate the JK flip flop characteristics table and realize T flip flop using JK flip flop.
(CO3) [Application]

