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PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING
END TERM EXAMINATION - JAN 2023

Semester : Semester V - 2020
Course Code : ECE3008
Course Name : Sem V - ECE3008 - VLSI Design
Program : B.Tech. Electronics and Communication Engineering

Date : 11-JAN-2023
Time : 9.30AM - 12.30PM
Max Marks : 100
Weightage : 50%

Instructions:
(i) Read all questions carefully and answer accordingly.
(ii) Question paper consists of 3 parts.
(iii) Scientific and non-programmable calculator are permitted.

PART A

ANSWER ALL THE FIVE QUESTIONSQ **5 X 2 = 10M**

1. There are various operators available in verilog HDL like Logical operator,Boolean Logical operator,Reduction Logical operator,Relational operators. Consider the following code X = 1010 and perform reduction AND operation on it.

(CO1) [Knowledge]

2. The logic element like an inverter reverses the applied input signal. In digital logic circuits, binary arithmetic & switching or logic function's mathematical manipulation are best performed through the symbols 0 & 1. Draw a Static CMOS Circuit for an "INVERTER".

(CO3) [Knowledge]

3. Transmission gates are parallel combination of pmos and nmos transistor with the gates connected to a complementary input. complete the following sentences.
When C="__" n and p device ____, Vin=0 or 1, Vo="Z" where „Z" is high impedance.
When C=" __" n and p device ____ , Vin=0 or 1, Vo=0 or 1 ,

(CO3) [Knowledge]

4. The transfer characteristic relates drain current (Id) response to the input gate-source driving voltage (Vgs) for a MOSFET . Draw the Graph of Vds Vs Id
Identify the various regions of operation of a N-MOSFET.

(CO2) [Knowledge]

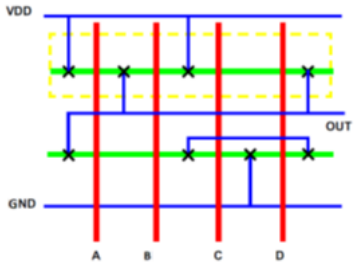
5. There are main three types of scaling stated as general scaling, constant field and constant voltage scaling. In general scaling state the scaling factor for idss.

(CO2) [Knowledge]

PART B

ANSWER ALL THE TWO QUESTIONS **2 X 15 = 30M**

6. Stick diagrams are helpful in sketching an initial layout of a CMOS-based circuit. Consider the following stick diagram and do the following:
(a) Draw the CMOS circuit implementation by showing both Pull-up and Pull-down networks.
(b) Identify the number of valid Euler's Paths and list them.



(CO3) [Comprehension]

7. A CMOS circuit consists of a pull-up network and a pull-down network. Draw the CMOS transistor network implementation of the Boolean expression: $F = \overline{DE + C(A+B)}$

(CO3) [Comprehension]

PART C

ANSWER ALL THE THREE QUESTIONS **3 X 20 = 60M**

8. A game is designed where inputs are chosed in decimal numbers varying from 0 to 7 but outputs are obtained in binary form. A user starts playing with this game designed such that if he press button I7 the output is obtained in binary form as 111, similarly for I5 as 101 and so on. If the user press two buttons at a time then the button with higher decimal notation would be chosen. Design the circuit for the defined scenario using Behavioural modelling style in Verilog And Write Its Truth Table Along With Expected Output Waveform.

(CO1) [Application]

9. The drain characteristics of a MOSFET are drawn between the drain current ID and the drain source voltage VDS. VGS also plays an important role to depict the region of operation and switch on the transistor. Compute the unknown values for the following numerical based questions.
a)The gate to source voltage of a nmos working with Vt=0.4 V is 0.9 V, while region of operation here is saturation region. The value of drain current is 1mA. Compute the value of ID when VGS=1.4v.
b)The drain of NMOS is shorted to gate. Vt=1V,if Id=1milli-amps at vgs=2V, find the value of Id at VGS=3V.

(CO2) [Application]

10. Digital inverter quality is often measured using the Voltage Transfer Curve (VTC), which is a plot of input vs. output voltage. From such a graph, device parameters including noise tolerance, gain, and operating logic-levels can be obtained. Ilustrate all the five cases pertaining to the VTC curve. Include the operating region for both transistors in the cases and explain it for values: Vth-0.4 V and Vdd=5v.

(CO3) [Application]

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