ROLL NO													

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

MAKEUP EXAMINATION – JAN 2023

Course Code: ECE215

Course Name: VLSI DESIGN

Program : B.Tech

Date: 27-JAN-2023

Time: 01:00 PM TO 04:00 PM

Max Marks: 100

Weightage: 50%

Instructions:

(i) ***Read the question carefully and answer all the questions***

Part A[Memory Recall Questions]

Answer all the Questions. Each Question carries TWO marks **(20Qx2M=40M)**

1.CMOS inverter has _____ distinct regions of operation which can be determined by plotting CMOS inverter current versus Vin. **(C.O.2)[**Knowledge Level]

a) three
b) four
c) two
d) five

2.If n-transistor conducts and has large voltage between source and drain, then it is in _____ region

(C.O.2)[Knowledge Level]

a) linear
b) saturation
c) non saturation
d) cut-off

3.If both the transistors are in saturation, then they act as _____so that the equivalent circuit is two _____ between Vdd and Vss. **(C.O.2)[**Knowledge Level]

a) current source
b) voltage source
c) divider
d) buffer

4. If βn = βp, then Vin = _____ which implies that the changeover between logic levels is symmetrically disposed about the point. **(C.O.3)[**Knowledge Level]

a) Vdd
b) Vss
c) 2Vdd
d) 0.5Vdd

5. Mobility is affected by the _____ and thus also depends on Vgs and the mobility of p-device and n-device are inherently unequal. **(C.O.2)[**Knowledge Level]

a) Transverse electric field
b) Vg
c) Vdd
d) Channel length

6. Under Gradual Channel Approximation (GCA), the depletion region in the bulk of the long channel MOSFET on application of a drain bias **(C.O.2)[**Knowledge Level]

a. Reduces as we move towards the drain end
b. Increases as we move towards the drain end
c. Remains constant
d. Has no relationship

7. In order to remove the body effect, the substrate of an n-channel enhancement mode MOSFET should be **(C.O.2)[**Knowledge Level]

a. Connected to the most positive bias
b. Connected to the most negative bias
c. Grounded
d. Floating

8. For a bulk MOSFET with aspect ratio of W/L and a depletion width of XD the analytical expression for gate-to-drain overlap capacitance (Cgd) is **(C.O.3)[**Knowledge Level]

a. Cgd = 2CoxWXD
b. Cgd = CoxXDW/2
c. Cgd = 2CoxXDWL
d. Cgd = CoxXDWL

9. A static CMOS Inverter is powered by a supply voltage of VDD. Assuming the pull-up and pull-down networks are equal and symmetric, which of the following statement are true **(C.O.3)[**Knowledge Level]

a. The switching threshold is VDD/2
b. The switching threshold is 2VDD
c. The switching threshold is VDD
d. The switching threshold is VDD/4

10. For a static CMOS, the output is high, then the state of the NMOS and PMOS are as follows

(C.O.3)[Knowledge Level]

a. NMOS on and PMOS non-linear
b. NMOS off and PMOS linear
c. NMOS off and PMOS non-linear
d. NMOS on and PMOS linear

11. In order to remove the body effect, the substrate of an n-channel enhancement mode MOSFET should be **(C.O.2)[**Knowledge Level]

a. Connected to the most positive bias
b. Connected to the most negative bias
c. Grounded
d. Floating

12. A bulk n-channel enhancement mode MOSFET is biased in the saturation region of operation, such that VDS> VGS – Vth. Vth is the threshold voltage. Taking into consideration Channel Length Modulation, the effective channel length is given as: **(C.O.2)[**Knowledge Level]

a. L'=L- Δ L
b. L'=L-2L
c. L'=L- µL
d. L'=L- ÜL

13. In constant field model, the scaling factor of switching energy per gate would be

(C.O.2)[Knowledge Level]

a. 1/βα^2
b. 1/ α^3
c. 1/ α^2
d. All of the mentioned

14. CMOS inverter has output impedence_____ **(C.O.3)[**Knowledge Level]

a. Moderate
b. Low
c. High
d. None

15. Reduction in power dissipation can be brought by **(C.O.3)[**Knowledge Level]

a. Increasing transistor area
b. Decreasing transistor area
c. Increasing transistor feature size
d. Decreasing transistor feature size

16. Pmos used as a pull up network because of **(C.O.3)[**Knowledge Level]

a. Pass week 0
b. Pass week 1
c. Pass strong 0
d. Pass strong 1

17. The source and drain regions are formed by diffusing n-type impurity, it gives rise to depletion region which extend in more lightly doped p-region. Thus Source and drain in an nMOS device are isolated by _____ **(C.O.2)[**Knowledge Level]

a) a single diode
b) two diodes
c) three diodes
d) four diodes

18. The condition for non saturated region is_____. In non saturation region, MOSFET acts as voltage source. Varying Vds will provide a significant change in drain current. **(C.O.2)[**Knowledge Level]

a) Vds = Vgs – Vt
b) Vgs lesser than Vt
c) Vds lesser than Vgs – Vt
d) Vds greater than Vgs – Vt

19. In enhancement mode the device is in non conducting mode, and its condition is _____

(C.O.2)[Knowledge Level]

a) Vds lesser than Vgs
b) Vgs lesser than Vds
c) Vgs = Vds = 0
d) Vgs = Vds = Vs = 0

20. MOS transistor structure is _____ **(C.O.2)[**Knowledge Level]

a) symmetrical
b) non symmetrical
c) semi symmetrical
d) pseudo symmetrical

Part B [Thought Provoking Questions]

Answer both the Questions. Each Question carries TEN marks. (3Qx10M=30M)

1. List the Port in Verilog. Write a Verilog Program using 4:1 Multiplexer. (C.O.NO.1) [Comprehension]

2. Design an 8:3 Priority encoder, write a Verilog code using behavioral description(if-else-statement) and verify its logic using its truth table. (C.O.NO.1) [Comprehension]

3.Explain VLSI Design flowchart which includes different types of processing step for IC Design. (C.O.NO.2) [Comprehension]

Part C [Problem Solving Questions]

Answer the Question. The Question carries FIFTEEN marks. (3Qx15M=30M)

1.Explain the steps of N-MOS fabrication with neat diagram. (C.O.NO.2) [Comprehension]

2. A typical CMOS inverter has the voltage transfer characteristics VTC curve as shown the figure
   i. Determine the Gain in region 2 and region 4
   ii. At region1 , both the Pmos and Nmos transistors are operated in
   iii. For calculating Switching threshold of an CMOS inverter the region of P and N transistors are

(C.O.NO.3) [Comprehension]