Roll No												

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

MAKE-UP EXAMINATION- JAN 2023

Course Code: ECE2002/ ECE2006

Course Name: Digital Electronics

Program & Sem: B. Tech - ECE

Date: 23/01/2023

Time: 09:30AM - 12:30PM

Max Marks: 100

Weightage: 50%

Instructions:

(i) Read the all questions carefully and answer accordingly.

(ii) Draw diagrams wherever necessary.

(iii) Use of a non-programmable scientific calculator is permitted.

Part A [Memory Recall Questions]

Answer all the Questions. Each question carries FIVE marks. (6Q x 5M= 30M)

1. State and prove De Morgan's theorem. (CO1, Knowledge)
2. Simplify F= X+XY'Z+XZ'+XYZ. (CO1, Knowledge)
3. A 8:1 MUX has_____inputs, _____output & _____selection lines. Write its truth table. (CO2, Knowledge)
4. Write the sum and carry output equations of full adder circuit and implement using logic gates. (CO2, Knowledge)
5. Write the characteristic equation and truth table of JK and D flip flops. (CO3, Knowledge)
6. Convert the decimal number $(168)_{10}$ to binary and hexadecimal number systems. (CO1, Knowledge)

Part B [Thought Provoking Questions]

Answer all Questions. Each question carries TEN marks. (4Q x 10M= 40M)

7. Mr. Joy intends to use a minimization technique called Kmap to reduce the Boolean expression f= ∑m(0,1,3,4,5,6,7,13,15). Help Mr. Joy implement the reduced expression using NAND gates only.

(C.O. No- 1) [Application Level]

8. Mr. Pranay intends to use a minimization technique called Kmap to reduce the Boolean expression f= πM(2,8,9,10,11,12,14). Help Mr. Pranany implement the reduced expression using NOR gates only.

(C.O. No- 1) [Application Level]

9. The basic function of a comparator is to compare the magnitudes of two binary quantities to determine the relationship of those quantities. Design the 2-bit comparator and implement it using logic gates.

(C.O. No- 2) [Application Level]

10. Higher order MUX/ DEMUX can be designed using lower order MUX/ DEMUX. Mr. Joel wants to design a 8X1 MUX. But he has only 2x1 MUX. Illustrate how a 8x1 MUX can be designed using 2x1 mux. Also show the design of 1x8 DEMUX using 1X2 DEMUX.

(C.O. No-2) [Application Level]

Part C [Problem Solving Questions]

Answer all the Questions. Each question carries FIFTEEN marks. (2Q x 15M = 30M)

11. Flip-flops and latches are used as data storage elements. In case of T flip flop, if the T input is high, the T flip-flop changes state ("toggles") whenever the clock input is strobed. If the T input is low, the flip-flop holds the previous value. Draw the logic symbol and circuit diagram, characteristic table and equation, excitation table for this flip flop.

(C.O. No-3) [Application Level]

12. Mr. Mathew plans to design a synchronous counter consisting of 4 JK flip-flops, wherein all the clocks are clocked at the same time by a common clock pulse. Design this 4-bit synchronous UP counter, explaining all the steps.

(C.O. No-3) [Application Level]