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## PRESIDENCY UNIVERSITY **BENGALURU**

#### SCHOOL OF ENGINEERING

### **MAKEUP EXAMINATION – JAN 2023**

Course Code: ECE 2007 Date: 23-JAN-2023

Course Name: Digital Design Time: 1:00PM to 4:00 PM

Programme : B. Tech Max Marks: 100

Weightage: 50%

#### Instructions:

as a D-Flipflop.

- Read Questions carefully and answer accordingly (i)
- Scientific and Non- programmable calculators are permitted (ii)
- (iii) This Examination mode is OFFLINE

## PART A (Memory Recall Questions)

Answ	er all the questions. Each question carries TWO Marks.	$[15Q \times 2M = 30M]$
1.	NAND & NOR GATES are called as	(CO.1) [B. Level: Knowledge]
2.	There are 16 input combinations in a digital system, how many m frame a Boolean Function?	inimum variables are required to (CO.1) [B. Level: Knowledge]
3.	Karnaugh map is used to simplify Boolean expression. How many map. Each product term of a group, w'.x.y'z and wx.y,z represents	cells are present in 4 variable k-
4.	In two input NAND gate one of the input goes to low level, then the	
5	An Encoder is a combinational logic circuit; it encodes certain set of	of inputs to outputs. In 2 <sup>N:</sup> N
	encoder the OUTPUT hasbit binary form.	(C.O.No.3) [Knowledge]
6	An adder is a combinational logic circuit whose output are sum and	carry. If two numbers, (6) <sub>10</sub> and
	(7) <sub>10</sub> are added using a full adder. At LSB position of both the numb	ers, will be the sum
	and will be the carry.	(C.O.No.2)[Knowledge]
7	A Half adder is an arithmetic circuit that adds two binary digits. It us	sesgate
	&gate.Its output are SUM & CARRY	(C.O.No.2) [Knowledge]
8	Multiplexer (MUX) is a Combinational logic circuit having single out	put line and many input lines.
	Four variable Boolean function can be implemented using (with the	minimal select lines)
	MUX.	(C.O.No.3) [Knowledge]
9	The outputs of a comparator irrespective of number of bits are	, and
10	Any number can be represented in various base systems. Find the	equivalent of (12) <sub>10</sub> in () <sub>2</sub> ,
	$(_{_{_{_{10}}}})_8$ , $(_{_{_{_{10}}}})_{10}$ and $(_{_{_{_{16}}}})_{16}$ ?	(CO.1) [B. Level: Knowledge]
11	A J-K flip flop is designed to overcome the shortcomings of S-	R latch. What is the major

difference between S-R latch and S-R Flipflop? How S-R Flipflop can be modified to work

(C.O.No.3) [Knowledge]

12	this, other input signals are present in MUX design called select lir	•
	hasinputs,output&selection lines .	(C.O.No.2)
	[Knowledge]	
13	For designing a 4 bit Asynchronous counter how many JK flipflop	are required? Which
	input combinations it produces no change state?	(C.O.No.3) [Knowledge]
14	T –flip flop is modified version ofFlip flop , In T	-flip flop ,for what input
	combinations it produces no change state?	(C.O.No.3) [Knowledge]
15	5 Digital circuits can be broadly classified as Combinational circuits,	and Sequential circuits.
	In a combinational circuit, the output depends on	(C.O.No.3) [Knowledge]

PART B (Thought Provoking Questions)

Answer any 4 Questions. Each Question carries 10 Marks. [4Q x 10M = 40M]

16 .Roy and his friends are interested to design a block that has 16 input lines and 1 output and that block is named as Multiplexer that performs reverse operation of a De-Multiplexer. Help them to build the block but they have only 2:1 MUX. Hence, implement 16:1 MUX using 2:1 MUX.

[CO2 B. Level: Comprehension]

- 17.Mr JOY wants to implement a warning buzzer when the following conditions apply:
  - Switches A, B, C are on.
  - Switches A and B are on but switch C is off
  - Switches A and C are on but switch B is off.
  - Switches C and B are on but switch A is off.
     Draw a truth table for this situation and obtain a Boolean expression for it. Minimize this expression and draw a logic diagram using NAND GATES.

[CO2 B. Level: Comprehension]

18. Find the Boolean expression in sum of product (SOP) from the given truth table and simplify the expression using K Map.

In	pι	ıts	Outputs
Α	В	$\circ$	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

[CO2 B. Level: Comprehension]

- a)Design and implement the simplified logic using LOGICAL GATES.
- b) Design and implement the simplified logic using 4:1 MUX [CO2 B. Level: Comprehension]

19. A comparator is a device that compares two bits, voltage or currents and outputs a digital signal indicating which is larger. Design a 1-Bit comparator with the help of truth table and obtain the logical expression for each case with the help of simplification method (K-map).

[CO2 B. Level: Comprehension]

# PART C (Problem Solving Questions) Answer any 2 the Questions. Each Question carries 15 Marks.

 $[2Q \times 15M = 30M]$ 

- 20. You can create a 3-input, 3-output circuit that maps one state in the *count* sequence to the next. Design synchronous 3 bit up counter using T flipflop.
  - a. Write excitation table of Flip Flop
  - b. Draw the state transition diagram and circuit state table.
  - c. Find a simplified equation using k map.
  - d. Create a circuit diagram

(C.O.No. 3) [Application]

- 21. In Boolean algebra, circuit minimization is the problem of obtaining the smallest logic circuit that represents a given Boolean function or truth table. Mr Joel is provided with Boolean function  $F=\Sigma m(0,1,4,7,9,13,15)$ 
  - a) Write whether the below expression is an SOP or POS expression and what is the full-form? Write whether the below expression is a min-term or max-term expression? How many variable K-map we need to simplify the below expression? Draw the K-map and simplify the above expression by showing all the steps.
  - b) Implement the simplified expression obtained in Part (b) using basic gates.
  - c) Implement the simplified expression obtained in Part (b) using NAND gates. .

(C.O.No. 2) [Application]

- 22. A sequential circuit refers to a special type of circuit where the outputs depend on a combination of both the present inputs as well as the previous outputs.
  - a) Discuss the comparison between Synchronous and Asynchronous circuits.
  - b)Design a 3-bit Asynchronous up-counter, how many flip flops required and mention the number of states using state diagram. (C.O.No. 2) [Application]