Roll No											

PRESIDENCY UNIVERSITY
BENGALURU

SET - A

SCHOOL OF ENGINEERING
END TERM EXAMINATION - JUN 2023

Semester : Semester II - 2022
Course Code : ECE2007
Course Name : Sem II - ECE2007 - Digital Design
Program : B.Tech - All Programs

Date : 21-JUN-2023
Time : 1.00PM - 4.00PM
Max Marks : 100
Weightage : 50%

Instructions:
(i) Read all questions carefully and answer accordingly.
(ii) Question paper consists of 3 parts.
(iii) Scientific and non-programmable calculator are permitted.
(iv) Do not write any information on the question paper other than Roll Number.

PART A

ANSWER ALL THE QUESTIONS **(5 X 2 = 10M)**

1. In Digital Electronics, we find two types of networks: Combinational Networks and Sequential Networks. Accordingly, Identify the category to which Binary Decoder belongs to _____? If the number of Inputs to a Binary decoder are 3, then the number of Outputs are _____ ?

(CO3,CO4) [Knowledge]

2. How many cells are present in a 2-variable K–map? Also, draw a template of a 2-variable K–map.

(CO2,CO1) [Knowledge]

3. A digital circuit is used for data selection, data routing, operation sequencing, waveform generation, logic function generation. Identify and draw the block diagram of the circuit, which accepts eight input data line and allows only one of them at a time to the output with the help of selection lines.

(CO5) [Knowledge]

4. A parity bit is added to data bits in order to provide error detection. For even parity, a parity bit is added to the data bits to make the total number of 1's in the data bits even. Draw the logic diagram of an even parity generator for data bits 0001.

(CO1,CO3) [Knowledge]

5. The Base-16 number system is used while fetching the data from a memory location in a computer system. The current data fetching is taking place at the **22E** memory location. What will that number be in the Base-10 number system if a user has to understand this number?

(CO1) [Knowledge]

PART B

ANSWER ALL THE QUESTIONS **(2 X 15 = 30M)**

6. A student wants to design a digital logic switching function which is described by the following Boolean Function in SoP, $F(A,B,C,D)=\sum m(1,3,4,11,12,13,14,15)$. But he has been provided with only 8x1 MUX. Guide the student to design the switching function using MUX only

(CO5) [Comprehension]

7. The advantage of using complements in digital design is to perform subtraction by making use of addition. Design a combinational logic circuit that considers the three values namely minuend, subtrahend, and borrow-in to generate the difference and borrow outputs.

(CO3) [Comprehension]

PART C

ANSWER ALL THE QUESTIONS **(3 X 20 = 60M)**

8. The shift register can shift the bits either towards the right or left. Illustrate the below-mentioned three shift registers.

(a) It is used in the receiver section before DAC (SIPO).
(b) Fastest one among all shift registers (PIPO) and
(c) The shift register allows serial input and produces serial output (SISO).

(CO5) [Application]

9. Let n=4 bit binary number. You have to implement a logical circuit to check if n is divisible by 3. Draw a truth table for this situation and obtain a Boolean expression for it using the design procedure. Minimize this expression and draw a logic diagram using

- Basic gates
- NAND gates

(CO2) [Application]

10. Natasha wants to start the race with the down count of 3 bits. To facilitate Natasha, Design 3-bit Synchronous DOWN counter using SR flip flop by identifying the truth table, state-diagram, state table, characteristic table, excitation table, Boolean expression to develop the Logic Diagram

(CO3,CO5) [Application]