Roll No											

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING
MID TERM EXAMINATION - APR 2023

Semester : Semester VI - 2020
Course Code : ECE3046
Course Name : Sem VI - ECE3046 - Low Power Vlsi Design
Program : ECE

Date : 15-APR-2023
Time : 2PM - 3.30PM
Max Marks : 60
Weightage : 30%

Instructions:
(i) Read all questions carefully and answer accordingly.
(ii) Question paper consists of 3 parts.
(iii) Scientific and non-programmable calculator are permitted.
(iv) Do not write any information on the question paper other than Roll Number.

PART A

ANSWER ALL THE QUESTIONS **(5 X 2 = 10M)**

1. In low-power applications, reducing power dissipation at different levels is an important one. Mention three parts that the designer can perform low power technique to reduce power dissipation
(CO1) [Knowledge]
2. The power gating is one of efficient method in dynamic power reduction. Describe power gating.
(CO1) [Knowledge]
3. The process of reducing channel length leads to short channel effects. What is hot electron effect?
(CO1) [Knowledge]
4. The SoI is the latest trend and device technology in lower-power type applications. Illustrate SoI.
(CO1) [Knowledge]
5. The body effect is a basic process of VTCMOS and MTCMOS. Describe body effect.
(CO1) [Knowledge]

PART B

ANSWER ALL THE QUESTIONS **(3 X 10 = 30M)**

6. (a) The number of devices per chip and the system performance has been improving exponentially over the last two decades. As the channel length is reduced, the performance improves, the power per switching event decreases, and the density improves. Describe scaling and different types. (5)

(b) The current between the source and drain of a MOSFET when the transistor is in a subthreshold region, or weak-inversion region. Explain in detail about subthreshold leakage current. (5)

(CO1) [Comprehension]

7. The rising demand for portable and even wearable electronic devices for communication, computing, and entertainment has necessitated longer battery life, lower power consumption, and lesser device weight.Discuss about VTCMOS power reduction technique.

(CO1) [Comprehension]

8. Drain-induced barrier lowering (DIBL) is a short-channel effect in MOSFETs referring originally to a reduction of threshold voltage of the transistor at higher drain voltages. Explain in detail about DIBL and Punch through.

(CO1) [Comprehension]

PART C

ANSWER ALL THE QUESTIONS **(2 X 10 = 20M)**

9. Power dissipation can be defined as the product of the total current supplied to the circuit and the total voltage loss or leakage current. When it comes to the portability of devices, power dissipation is an unavoidable constraint. Describe switching power dissipation of CMOS circuit.

(CO1) [Application]

10. An important step to design a digital system is gate level simulation. Explain in detail the need for gate level simulation

(CO2) [Application]