Roll No											

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING
MID TERM EXAMINATION - MAY 2023

Semester : Semester VI - 2020
Course Code : ECE3046
Course Name : Sem VI - ECE3046 - Low Power Vlsi Design
Program : ECE

Date : 19-MAY-2023
Time : 10.30AM - 12.00PM
Max Marks : 60
Weightage : 30%

Instructions:
(i) Read all questions carefully and answer accordingly.
(ii) Question paper consists of 3 parts.
(iii) Scientific and non-programmable calculator are permitted.
(iv) Do not write any information on the question paper other than Roll Number.

PART A

ANSWER ALL THE QUESTIONS **(5 X 2 = 10M)**

1. In low-power applications, reducing power dissipation at different levels is an important one. Mention three parts that the designer can perform low power technique to reduce power dissipation
(CO1) [Knowledge]
2. The SoI technology supports different types of low-power applications such as RFID and bio medical implanted devices. Mention the advantages of SoI
(CO1) [Knowledge]
3. For an increasing number of components, the channel length is reduced. It may become short-channel devices. Define the short-channel device?
(CO1) [Knowledge]
4. The oxide thickness plays important role in reducing threshold voltage of low-power design. Illustrate equivalent oxide thickness.
(CO1) [Knowledge]
5. Clock gating is a traditional technique for reducing power dissipation of the circuit in low-power design. Illustrate clock gating.
(CO1) [Knowledge]

PART B

ANSWER ALL THE QUESTIONS **(3 X 10 = 30M)**

6. (a) The aim of low-power VLSI design is to minimize the individual components of power as much as possible, hence decreasing the total power consumption. Explain in detail need for low power design. (5)
(b) The nMOS and pMOS transistors used in a CMOS logic gate generally have nonzero reverse leakage and sub-threshold currents. But in a practical scenario there exists a leakage current. Describe the reverse diode leakage current. (5)

(CO1) [Comprehension]

7. (a) Glitch power comes under dynamic dissipation in the circuit and is directly proportional to switching activity. Glitch power dissipation is 20%–70% of total power dissipation and hence glitching should be eliminated for low-power design. Descrbe glitch power dissipation with a suitable example. (5)
(b) The sizing of the transistor can be done using RC delay approximation. The RC Delay Model helps in delay estimation CMOS circuit.
Realize Y=(D+(A*(B+C)))' in CMOS and evaluate the sizing of the transistor. (5)

(CO1) [Comprehension]

8. Low-power designs will reduce the power in high-end systems with huge integration density and thus improve the speed of operation. Multiple-Threshold CMOS (MTCMOS) Circuits are an efficient technique that will enable devices with high computation. Describe the MTCMOS technique.

(CO1) [Comprehension]

PART C

ANSWER ALL THE QUESTIONS **(2 X 10 = 20M)**

9. SPICE is open-source software that simulates the operating conditions of analog circuits.
(a) Illustrate transient analysis of CMOS Inverter. (7)
(b) (i) What is SPICE? (ii) Differentiate LTSPICE and HTSPICE. (3)

(CO2) [Application]

10. The short-circuit energy dissipation results due to a direct path current flowing from the power supply to the ground during the switching of a static CMOS gate. Explain in detail about short circuit power dissipation in CMOS circuit.

(CO1) [Application]