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**PRESIDENCY UNIVERSITY
BENGALURU**

**SCHOOL OF ENGINEERING
MID TERM EXAMINATION - APR 2023**

Semester : Semester II - 2022

Course Code : ECE2007

Course Name : Sem II - ECE2007 - Digital Design

Program : All Program

Date : 18-APR-2023

Time : 9:30AM - 11AM

Max Marks : 50

Weightage : 25%

Instructions:

- (i) Read all questions carefully and answer accordingly.
- (ii) Question paper consists of 3 parts.
- (iii) Scientific and non-programmable calculator are permitted.
- (iv) Do not write any information on the question paper other than Roll Number.

PART A

ANSWER ALL THE QUESTIONS

(5 X 2 = 10M)

1. The binary, decimal, and hexadecimal number systems are also known as Base-2, Base-10, and Base-16 number systems. Convert the decimal number 61234 to its equivalent hexadecimal number and binary number.
(CO1) [Knowledge]
2. In a computer while fetching the data from one memory location, hexadecimal number system is used. At an instance, the current data fetching is happening at 11C location. If a human has to understand this number, what will that number be?
(CO1) [Knowledge]
3. Boolean algebra specifies various laws for simplification of logical expression.
In Boolean Algebra: $A' + B' + C' = (A \cdot B \cdot C)'$ is known as _____.
In Boolean Algebra: i. $A + A'B =$ _____ ii. $A + A' =$ _____ iii. $A + 1 =$ _____ iv. $A \cdot A' =$ _____ v. $A \cdot A =$ _____
(CO1) [Knowledge]
4. The minimum number of NAND gates required to implement the Boolean expression $f = A'B + AB' + AB$ is _____.
(CO1,CO2) [Knowledge]
5. A designer can design a half-adder circuit using multiple NAND gates only. How many NAND gates are required to design a half-adder circuit?
(CO3) [Knowledge]

PART B

ANSWER ALL THE QUESTIONS

(4 X 5 = 20M)

6. Mr. Joy wants to implement a warning buzzer when the following conditions apply:

- Switches A, B, C are on.
- Switches A and B are on but switch C is off
- Switches A and C are on but switch B is off.
- Switches B and C are on but switch A is off.

Write the truth table for this situation and obtain a Boolean expression for it. Minimize this expression and draw a logic diagram using NAND gates.

(CO2) [Comprehension]

7. Design a 4-bit digital system that will identify the parity of the data being transmitted. The transmitted data can vary between 0 and 9. The data is transmitted using BCD format, which means the numbers greater than '1001' are invalid. The output is '1' for even parity and '0' for odd parity. Derive the minimized expression using K-maps.

(CO2) [Comprehension]

8. The designer can design the full adder using two half adders and one OR gate. Design the full adder circuit using half adders and OR gate.

(CO3,CO1) [Comprehension]

9. The universal gates namely NAND and NOR are utilized to design any digital circuits since they are economical and easy to fabricate. Implement the combinational circuit that subtracts three bits using the universal gates.

(CO3) [Comprehension]

PART C

ANSWER ALL THE QUESTIONS

(2 X 10 = 20M)

10. Answer the following questions related to the function $f(A,B,C,D)$ as defined by its minterms

$$f(A,B,C,D) = \sum m(7,9,11,12,13,14,15)$$

- a) Enter the minterms and maxterms on a suitable K-map and deduce the minimal canonical form for $f(A,B,C,D)$.
- b) Implement the above function using only basic gates
- c) Implement the above function using only 2-input NAND gates

(CO2) [Application]

11. While performing a task using binary arithmetic a student is stuck at a module which computes the difference between $A=0$ and $B=1$ considering subtraction as $A-B$. Draw the circuit for the above scenario and implement it using only NAND gates. Draw the required truth table and state simplified equations for the output.

(CO3) [Application]