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**PRESIDENCY UNIVERSITY  
BENGALURU**

**SET - B**

**SCHOOL OF ENGINEERING  
MID TERM EXAMINATION - APR 2023**

**Semester :** Semester II - 2022

**Course Code :** ECE2007

**Course Name :** Sem II - ECE2007 - Digital Design

**Program :** ALL PROGRAMS

**Date :** 18-APR-2023

**Time :** 9.30AM - 11AM

**Max Marks :** 50

**Weightage :** 25%

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**Instructions:**

- (i) Read all questions carefully and answer accordingly.
  - (ii) Question paper consists of 3 parts.
  - (iii) Scientific and non-programmable calculator are permitted.
  - (iv) Do not write any information on the question paper other than Roll Number.
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**PART A**

**ANSWER ALL THE QUESTIONS**

**(5 X 2 = 10M)**

1. A logic gate is a device that acts as a basic building block for digital logic circuits. Draw the logic symbol, write the logic expression, and write the truth table of an Exclusive-NOR gate.  
(CO1) [Knowledge]
2. A digital system can understand a positional number system only where there are a few symbols called digits and these symbols represent different values depending on the position they occupy in the number. Calculate and fill in the blanks with equivalent values for the following.
  - i. Binary equivalent of a given octal number 377 is \_\_\_\_\_?
  - ii. Hexadecimal equivalent of a given octal number 377 \_\_\_\_\_?(CO1) [Knowledge]
3. Each term in canonical form contains all possible literals. Convert the given Boolean expression  $Y=A+BC'+AB+A'BC$  into canonical form.  
(CO1) [Knowledge]
4. A 3-variable K-map contains \_\_\_\_\_ cells . Write a general template of K map for the same for the given minterms.  
(CO1,CO2) [Knowledge]
5. A half subtractor performs subtraction of only 2 binary bits with borrow and difference bit as output. It can be represented using basic logic gates and special gates or only universal logic gates. Design the half subtractor circuit using XOR and basic gates.  
(CO3) [Knowledge]

## PART B

### ANSWER ALL THE QUESTIONS

(4 X 5 = 20M)

6. Mr. Mathew intends to use a minimization technique called K-map to reduce the Boolean expression  $f = \sum m(0,1,2,4,7,8,9,10,12) + d(3,6,13,15)$ . Help Mr. Mathew implement the reduced expression using NAND gates only.
- (CO2) [Comprehension]
7. Design a digital system that will count the number of 1's available in the input data. The data has only 4-bits and represented using the 8-4-2-1 code. The output follows a set of rules: (i) If the number of 1's in the input is less than 2, then the output is 0; (ii) If the number of 1's in the input is greater than 2, then the output is 1; (iii) If the number of 1's in the input is equal to 2, then the output is don't care. For this system, derive the minimized expression using K-maps.
- (CO2) [Comprehension]
8. A group of 4 friends Arushi, Apoorva, Raghav and Rohit went to Goa for picnic (obviously before COVID situation). As Goa is famous for water sports they decided to go for Scuba Diving. As photographs help preserve good memories, they decided to capture these important moments. The photographer agreed to click picture if
1. Arushi will go for scuba diving
  2. Apoorva and Raghav go at the same time for scuba diving
  3. Rohit and Raghav go at the same time for scuba diving
  4. Apoorva, Raghav, Rohit go at the same time for scuba diving.

Analyse the given scenario using truth table and verify the correctness of the design using Basic gates only.

(CO3,CO1) [Comprehension]

9. The advantage of using complements in digital design is to perform the subtraction by making use of addition. Design a combinational circuit that considers the three values namely minuend, subtrahend and borrow-in to generate the difference and borrow-out.

(CO3) [Comprehension]

## PART C

### ANSWER ALL THE QUESTIONS

(2 X 10 = 20M)

10. Let  $n = 4$ -bit binary number. You have to implement a Logical circuit to check  $n \div 3$ . Draw a truth table for this situation and obtain a Boolean expression for it using the design procedure. Minimize this expression and draw a logic diagram using
- a) Basic gates
  - b) NAND gates
- (CO2) [Application]
11. A full adder takes two binary numbers plus a carry or overflow bit. The output is a sum and another carry bit. Full adders are made from XOR, AND, and OR gates in hardware. Design a full adder circuit using NAND gates.
- (CO3) [Application]