Roll No											

PRESIDENCY UNIVERSITY
BENGALURU

SET - B

SCHOOL OF ENGINEERING
END TERM EXAMINATION - JUN 2023

Semester : Semester II - B.Tech ECE - 2022
Course Code : ECE2007
Course Name : Sem II - ECE2007 - Digital Design
Program : B.Tech. Electronics and Communication Engineering

Date : 21-JUN-2023
Time : 1.00PM - 4.00PM
Max Marks : 100
Weightage : 50%

Instructions:
(i) Read all questions carefully and answer accordingly.
(ii) Question paper consists of 3 parts.
(iii) Scientific and non-programmable calculator are permitted.
(iv) Do not write any information on the question paper other than Roll Number.

PART A

ANSWER ALL THE QUESTIONS **(5 X 2 = 10M)**

1. The Base-2, Base-10, and Base-16 number systems are also known as binary, decimal, and hexadecimal number systems. Convert the Base-10 number 42145 to its equivalent Base-2 number and Base-16 number.

(CO1) [Knowledge]

2. Digital circuits are classified as combinational and sequential circuits. Using a simple schematic block diagram, show the difference between a combinational logic circuit and a sequential logic circuit.

(CO3,CO4) [Knowledge]

3. In the canonical form, all possible literals are present in each term of the Boolean expression. Convert the following Boolean expression Y=P+QR′+PQ+P′QR into canonical form.

(CO2,CO1) [Knowledge]

4. In a Priority Encoder, D0, D1 & D2 are high means what is the encoded value of an 8 into 3 line Encoder?

(CO5) [Knowledge]

5. Given the Boolean expression f= P'Q+ PQ'+PQ. How many minimum number of NAND gates are required to implement the given Boolean expression?

(CO1,CO3) [Knowledge]

PART B

ANSWER ALL THE QUESTIONS **(2 X 15 = 30M)**

6. The advantage of using complements in digital design is to perform subtraction by making use of addition. Design a combinational logic circuit that considers the three values namely minuend, subtrahend, and borrow-in to generate the difference and borrow outputs.

(CO3) [Comprehension]

7. Leela wants to create a situation to dictate when the latch can and cannot latch. For this, she extends an SR latch with an *Enable* line which must be driven high before data can be latched. Even though a control line is now required, the SR latch is not synchronous, because the inputs can change the output if the enable line is held high at length. When the *Enable* input is low, then the outputs remain latched to the previous data. Only when the enable input is high can the state of the latch change. Draw a truth table to discuss this scenario. Identify the latch in the discussion. Implement this using NAND gates only. Discuss the significant differences between a latch and a flip-flop.

(CO5) [Comprehension]

PART C

ANSWER ALL THE QUESTIONS **(3 X 20 = 60M)**

8. Answer the following questions related to the function f(A,B,C,D) as defined by its minterms f(A,B,C,D)= Σ m(0,1,3,4,5,6,7,13,15)
   a) Enter the minterms and maxterms on a suitable K-map and deduce the minimal canonical form for f(A,B,C,D).
   b) Implement the above function using only basic gates
   c) Implement the above function using only NAND gates

(CO2) [Application]

9. Consider a case where the designer has only JK flipflop available with him and he is assigned a task to design a D flipflop using JK flipflop. Explain the conversion from JK to D flipflop using Excitation tables.

(CO5) [Application]

10. A comparator used to compare two binary numbers each of two bits is called a 2-bit Magnitude comparator. It consists of four inputs and three outputs to generate less than, equal to, and greater than between two binary numbers. Generate the truth table for A is equal to B and draw the logic circuit diagram for 2-bit magnitude comparator using NAND gates.

(CO3,CO5) [Application]