Roll No											

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING
MID TERM EXAMINATION - OCT 2023

Semester : Semester III - 2022
Course Code : ECE2002
Course Name : Sem III - ECE2002 - Digital Electronics
Program : B.TECH

Date : 30-OCT-2023
Time : 2:00PM - 3:30PM
Max Marks : 50
Weightage : 25%

Instructions:
(i) Read all questions carefully and answer accordingly.
(ii) Question paper consists of 3 parts.
(iii) Scientific and non-programmable calculator are permitted.
(iv) Do not write any information on the question paper other than Roll Number.

PART A

ANSWER ALL THE QUESTIONS **(5 X 2 = 10M)**

1. The Exclusive NOR (EX-NOR or XNOR) gate is one of the arithmetic gates. Write the truth table and logical expression of an Exclusive NOR gate.

(CO2) [Knowledge]

2. The hexadecimal number system is also called as Base-16 system. List all the hexadecimal numbers.

(CO2) [Knowledge]

3. ---------- number of 'NAND' gates are required to realize the below function:

$F = (\overline{X} + \overline{Y})(W + Z)$

(CO1) [Knowledge]

4. The NAND gate and NOR gate are called Universal gates because they can perform all the three essential functions of AND, OR, and NOT gates. Implement AND, OR, and NOT gates using only NAND gates.

(CO2) [Knowledge]

5. The result of an experiment is 11011.101. Convert the value into the corresponding decimal number.

(CO1) [Knowledge]

PART B

ANSWER ALL THE QUESTIONS **(2 X 10 = 20M)**

6. a) A parity bit is added to data bits in order to provide error detection. For even parity, a parity bit is added to the data bits to make the total number of 1's in the data bits even. Draw the logic diagram of an even parity generator for data bits 0001.
b) A parity bit is added to data bits in order to provide error detection. For odd parity, a parity bit is added to the data bits to make the total number of 1's in the data bits odd. Draw the logic diagram of an odd parity generator for data bits 0101.

(CO1) [Comprehension]

7. Let n= 4-bit binary number. You have to implement a logical circuit to check **n ÷ 3**. Draw a truth table for this situation and obtain a Boolean expression for it. Minimize this expression and draw a logic diagram using basic gates and NAND gates only.

(CO2) [Comprehension]

PART C

ANSWER THE FOLLOWING QUESTION **(1 X 20 = 20M)**

8. Combinational circuit output at any time depends on the present inputs.
a) Is the subtractor a combinational circuit? Justify with the help of the truth table.
b) Implement half subtractor with logic gates.
c) Write the truth table for full subtractor and implement it using logic gates.

(CO2) [Application]