Roll No											

PRESIDENCY UNIVERSITY
BENGALURU

SET A

SCHOOL OF ENGINEERING
END TERM EXAMINATION - JAN 2024

Semester : Semester III - 2022
Course Code : ECE2002
Course Name : Digital Electronics
Program : B.Tech.

Date : 04-JAN-2024
Time : 9:30AM - 12:30 PM
Max Marks : 100
Weightage : 50%

Instructions:
(i) Read all questions carefully and answer accordingly.
(ii) Question paper consists of 3 parts.
(iii) Scientific and non-programmable calculator are permitted.
(iv) Do not write any information on the question paper other than Roll Number.

PART A

ANSWER ALL THE QUESTIONS **5 X 2M = 10M**

1. Boolean algebra is a branch of mathematics that deals with logical operations on binary variables. The variables are represented as binary numbers, where 1 represents true and 0 represents false. Simplify the logical expression $\overline{(A + \bar{B})(C + \bar{D})}$

(CO2) [Knowledge]

2. Write the sum output and carry output equations of a full adder circuit.

(CO2) [Knowledge]

3. NOR gates are a type of universal gates and can be used to build any logic diagram. Design (logic diagram) an active high SR latch using NOR gates.

(CO3) [Knowledge]

4. NAND gates are a type of universal gates and can be used to build any logic diagram. Write the truth table of an active low S'R' latch using NAND gates.

(CO3) [Knowledge]

5. The output of an experiment is found to be 0000 0000 0000 0001. Represent the same using hexadecimal number system.

(CO3) [Knowledge]

PART B

ANSWER ALL THE QUESTIONS **5 X 10M = 50M**

6. Demultiplexers are also known as data distributors. Design a 1x8 demultiplexer using several 1x2 demultiplexers.

(CO2) [Comprehension]

7. A full subtractor is a combinational circuit that performs subtraction of two bits, one is minuend and other is subtrahend, taking into account borrow of the previous adjacent lower minuend bit whereas a half subtractor is a digital logic circuit that performs binary subtraction of two single-bit binary numbers a minuend bit and a subtrahend bit. Implement full subtractor using two half subtractors and one OR gate.

(CO2) [Comprehension]

8. With the help of D flipflops explain how the Serial Input Serial Output (SISO) shift register stores the number 1111.

(CO3) [Comprehension]

9. A digital system is to be designed in which the week of the month is given as input in three-bit form. The day Monday is represented as '000', Tuesday as '001' and so on. The output of the system should be '1' corresponding to the input of the day containing “t” letter or otherwise it is '0'. If don’t care exist then consider the excess numbers in the input as don't care conditions for system of three variables (x,y,z). Implement the simplified logic using a) basic gates and b) NAND gates only.

(CO4) [Comprehension]

10. A full subtractor can be made of 2 half subtractors. Is the statement true. Justify with the help of truth tables and logic diagrams.

(CO4) [Comprehension]

PART C

ANSWER ALL THE QUESTIONS **2 X 20M = 40M**

11. The priority encoder is another type of combinational circuit like a binary encoder, except that it generates an output code based on the highest prioritized input. Priority encoders are used extensively in digital and computer systems as microprocessor interrupt controllers, where they detect the highest priority input. Draw the truth table and logic circuit diagram using logic gates for 8 inputs and 3 output lines and write the encoded output (3 bits) if the inputs (8 bits) are 11111001

(CO4) [Application]

12. Almost all traffic signals carry a down counter to indicate the remaining time before red/green lights are turned off. Design a 3-bit down counter using JK flipflops.

(CO5) [Application]