Roll No											

PRESIDENCY UNIVERSITY
BENGALURU

SET B

SCHOOL OF ENGINEERING
END TERM EXAMINATION - JAN 2024

Semester : Semester V - 2021
Course Code : ECE3008
Course Name :VLSI Design
Program : B.Tech.

Date : 05-JAN-2024
Time : 9:30AM - 12:30 PM
Max Marks : 100
Weightage : 50%

Instructions:
(i) Read all questions carefully and answer accordingly.
(ii) Question paper consists of 3 parts.
(iii) Scientific and non-programmable calculator are permitted.
(iv) Do not write any information on the question paper other than Roll Number.

PART A

ANSWER ALL THE QUESTIONS **5 X 2M = 10M**

1. Verilog HDL is used in the design and verification of digital circuits at the register-transfer level (RTL) of abstraction. Illustrate RTL in Verilog HDL.
(CO1) [Knowledge]
2. Determine the drain current for saturation region is $V_T = 1.05V, V_{GS} = 4V, k = \beta/2 = 0.4 * 10^{-3}$
(CO1) [Knowledge]
3. Current in the MOSFET is a function of gate-to-source voltage and drain-to-source voltage. What are the current equations for MOSFET?
(CO2) [Knowledge]
4. VLSI circuits are found in a variety of places, including your computer, automobile, digital camera, cell phones, and so on. List and explain two fabrication steps in VLSI based transistors.
(CO2) [Knowledge]
5. CMOS inverter includes one PMOS and one NMOS transistor. What is the switching threshold in a CMOS inverter?
(CO1,CO2) [Knowledge]

PART B

ANSWER ALL THE QUESTIONS **5 X 10M = 50M**

6. The VLSI design flow is a complex and iterative process that involves collaboration among designers, verification engineers, and physical designers. Draw the VLSI design flow diagram and describe it.
(CO3) [Comprehension]

7. Multiplexer is a universal element in digital circuits. Write a Verilog HDL code for 4:1mux in all three modelling.

(CO4) [Comprehension]

8. The threshold voltage in a MOSFET is defined as the minimum voltage required for the device to start conducting. Write the Threshold voltage expression and indicate each parameter. Mention the equation if non-zero substrate voltage is applied.

(CO3) [Comprehension]

9. MOS transistors suffer from unwanted parasitic effects. One such problem in MOSFET is latch up. With a neat figure explain latch up and mention its prevention techniques.

(CO3) [Comprehension]

10. The DC analysis of the inverter is a function of the output voltage (Vout) with respect to the input voltage (Vin). Describe DC analysis of CMOS inverter.

(CO3,CO4) [Comprehension]

PART C

ANSWER ALL THE QUESTIONS **2 X 20M = 40M**

11. (a) CMOS is the semiconductor technology used in most of today's digital circuits. Realize the Boolean function $F = \overline{A + \overline{(\overline{B} + CD)}}$ in CMOS technology. (7)
(b) Stick diagrams convey layer information through color codes. Design two input NOR gates in CMOS Technology and draw the stick diagram with Euler's graph. (8)
(c) Design rules represent a tolerance that ensures a very high probability of correct fabrication. Illustrate Well rules in Layout design. (5)

(CO5) [Application]

12. (a) PTL (Pass Transistor Logic) is an area efficient technology in VLSI. Implement two input AND, OR, NAND, and EX-OR gates using PTL and illustrate voltage degradation of pass transistors when connected in series. (14)
(b) Dynamic Random Access Memory (DRAM) uses only one transistor to store one bit of information. Explain in detail about DRAM-1T with a neat diagram. (6)

(CO5) [Application]