PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING
MID TERM EXAMINATION - OCT 2023

Semester : Semester V - 2021
Course Code : ECE3008
Course Name : Sem V - ECE3008 - VLSI Design
Program : B. TECH

Date : 31-OCT-2023
Time : 11:30AM - 1:00PM
Max Marks : 50
Weightage : 25%

Instructions:
(i) Read all questions carefully and answer accordingly.
(ii) Question paper consists of 3 parts.
(iii) Scientific and non-programmable calculator are permitted.
(iv) Do not write any information on the question paper other than Roll Number.

PART A

ANSWER ALL THE QUESTIONS   (5 X 2 = 10M)

1. . The Verilog HDL is used for designing hardware and for creating test entities to verify the behaviour of a piece of hardware. Define module in Verilog HDL.

    (CO1) [Knowledge]

2. The digital circuits are verified by using different data types. List out the various data types in Verilog HDL.

    (CO1) [Knowledge]

3. The different operators are used in Verilog HDL to implement gates and functions. Differentiate the operators == and ===.

    (CO1) [Knowledge]

4. Very Large-scale integration (**VLSI**) is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip. List out the advantages of VLSI design.

    (CO1) [Knowledge]

5. The various steps are involved in IC fabrication. Illustrate CVD in IC fabrication processes.

    (CO2) [Knowledge]

PART B

ANSWER ALL THE QUESTIONS   (2 X 10 = 20M)

6. There are two types of circuits in digital design such as combinational and sequential circuits. Write a Verilog HDL code for a 3-to-8-line decoder and SR FF.

    (CO1) [Comprehension]

7. The counter is designed by using flip flops. Write a Verilog HDL code for a 4-bit binary counter and D-FF.

(CO1) [Comprehension]

PART C

ANSWER THE FOLLOWING QUESTION **(1 X 20 = 20M)**

8. . (i) The importance of CMOS in semiconductor technology is its low power dissipation and low operating currents. Its manufacturing requires fewer steps as compared to the Field Effect Transistors and Bipolar Junction transistors. Write a short note on the CMOS N-well process. (12)

(ii) The Gajski-Kuhn Y-chart is a model, which captures the considerations in designing semiconductor devices. Discuss the Gajski-Kuhn Y chart model. (8)

(CO1,CO2) [Application]