Roll No											

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING
MID TERM EXAMINATION - OCT 2023

Semester : Semester VII - 2020
Course Code : ECE3048
Course Name : Sem VII - ECE3048 - Fpga Design for Embedded Systems
Program : B. TECH

Date : 31-OCT-2023
Time : 2:00PM - 3:30PM
Max Marks : 60
Weightage : 30%

Instructions:
(i) Read all questions carefully and answer accordingly.
(ii) Question paper consists of 3 parts.
(iii) Scientific and non-programmable calculator are permitted.
(iv) Do not write any information on the question paper other than Roll Number.

PART A

ANSWER ALL THE QUESTIONS **(5 X 2 = 10M)**

1. The FPGA devices are part of Programable logic family. Explain with block diagram the basic classification of programmable logic devices.

(CO1) [Knowledge]

2. Quartus prime tool is used for designing and synthesizing the HDL code for various FPGA devices. If you have been asked to design a half adder using schematic way. List the steps you will follow to generate the output ?

(CO1) [Knowledge]

3. Programable devices are evolve and are becoming essential part of electronics hardware industry. The most popular family of programable devices are SPLD and CPLD devices. Explain with minimum two points how they are different from each other ?

(CO1) [Knowledge]

4. When it comes developing product for embedded world many options are available such as Designer has to do very wise of the platform to achieve time to market window. List all the other options with their correct names in detail.

(CO1) [Knowledge]

5. Quartus prime is a platform where FPGA boards are programmed using various methods like schematics, Verilog/VHDL,FSM etc. List the names of two FPGA boards that are available in 17-.1 version of Quartus prime?

(CO1) [Knowledge]

PART B

ANSWER ALL THE QUESTIONS **(4 X 5 = 20M)**

6. In order to achieve market to window a correct form of sales three popular devices FPGA,ASIC and CPLD are available . Company engineers have to make a tough choice among them to select for their final implementation, based on following criteria Best use for ,customization, Performance and development time. Give detail chart of above three devices with following point as reference and differentiate them.

(CO1) [Comprehension]

7. Verilog allows us to use three different styles of modelling behavioural, dataflow and structural . Write a Verilog code for designing a full adder using structural of modelling?

(CO1) [Comprehension]

8. Verilog allows us to use three different styles of modelling behavioural, dataflow and structural . Write a Verilog code for designing a full adder using behavioural style of modelling?

(CO2) [Comprehension]

9. Verilog allows us to use three different styles of modelling behavioural, dataflow and structural . Write a Verilog code for designing a Multiplexer using dataflow style of modelling?

(CO2) [Comprehension]

PART C

ANSWER ALL THE QUESTIONS **(2 X 15 = 30M)**

10. EDA tools help to create VLSI design in reality and also make it an easy job to handle the Timing constraints and RTL design. These tools need to follow a systematic design flow of to achieve great design. If you are a VLSI designer and you have been asked to create a prototype of the device,

1. What will be your choice of implementation FPGA or ASIC or any other device [1]
2. Name the popular devices that are compatible with the Quartus prime tool free version [2]
3. Name the EDA tool used in Quartus PrimeNA to visualize the output of the design [1]
4. List one method that can be used to create your VLSI design in Quartus Prime [1]
5. Discuss the entire VLSI design flow that can be used to implement VLSI design [10]

(CO1) [Application]

11. FPGA has lot of development in terms of internal components such as RAM ,DSP blocks CLB are the key role players in the popularity of FPGA . As a designer.

1. Identify the components CLB.[4]
2. Explain how F=AB+CD’ can be implemented in CLB [10]
3. What size LUT will be used to implement the equation[1]

(CO2) [Application]