Roll No											

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING
MID TERM EXAMINATION - OCT 2023

Semester : Semester III - 2022
Course Code : ECE2007
Course Name : Sem III - ECE2007 - Digital Design
Program : B. TECH

Date : 31-OCT-2023
Time : 11:30AM - 1:00PM
Max Marks : 50
Weightage : 25%

Instructions:
(i) Read all questions carefully and answer accordingly.
(ii) Question paper consists of 3 parts.
(iii) Scientific and non-programmable calculator are permitted.
(iv) Do not write any information on the question paper other than Roll Number.

PART A

ANSWER ALL THE QUESTIONS **(5 X 2 = 10M)**

1. There are 8 input combinations in the truth table of digital system .State the number of input variables for framing a standard form Boolean expressions? Also draw K map template for the same

(CO1) [Knowledge]

2. The Boolean Algebra specifies various laws for simplification of logic expression the Boolean Law A+A'B= _____.

(CO1) [Knowledge]

3. Any number can be represented in various base systems. Find the equivalent of (12)10 in (___)2, (___)8, (___)16 and (___)BCD?

(CO1) [Knowledge]

4. A comparator is a device that compares two bits, voltage or currents and outputs a digital signal indicating which is larger. Design a 1-Bit comparator with the help of truth table and obtain the logical expression for each case with the help of simplification method (K-map).

i)Implement Using Logical Gates
ii) Using NAND gates.

(CO2) [Knowledge]

5. A Half Adder is an arithmetic circuit that adds two binary digits .It uses _____ gate & _____gate for computing SUM and CARRY output respectively.

(CO2) [Knowledge]

PART B

ANSWER ALL THE QUESTIONS **(2 X 10 = 20M)**

6. A combinational logic circuit has 4 inputs, the output will be high only when the majority of the inputs are high. Draw a truth table for this situation and obtain a Boolean expression for it. Minimize this expression and draw a logic diagram using basic gates and NAND gates only

(CO1) [Comprehension]

7. The input to combinational logic circuit is a 4 bit binary number. Derive the truth table and implement using basic gates and NAND gates only when Output y=1 if the input binary number is 5 or less than 5.

(CO2) [Comprehension]

PART C

ANSWER THE FOLLOWING QUESTION **(1 X 20 = 20M)**

8. Implement a warning buzzer when the following conditions apply:

- Switches A, B and C are off.
- Switches A and B are off but switch C is on.
- Switches A and C are off but switch B is on.
- Switches C and B are off but switch A is on.

Draw a truth table for the complement of this situation and obtain a Boolean expression for it. Minimize this expression and draw a logic diagram using a) basic gates and b) NAND gates only.

(CO2) [Application]