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**Presidency University**

**Bengaluru**

**SCHOOL OF ENGINEERING**

**MAKE UP EXAMINATION JULY 2024**

**Course Code**: ECE2007

**Course Name**: DIGITAL DESIGN

**Program** : B.Tech.

**Date**: 22-07-2024

**Time**: 1:30 PM to 4:30PM

**Max Marks**: 100

**Weightage**: 50%

**Instructions:**

1. *Read all the questions carefully and answer accordingly.*
2. *Question paper consists of 3 parts.*
3. *Scientific and non-programmable calculator are permitted.*
4. *Do not write any information on the question paper other than Roll Number.*

**Part A [Memory Recall Questions]**

**Answer all the Questions. Each question carries two marks. (10Qx2M= 20M)**

**1.** Convert 10510 to a binary number system. [2M] (C.O.No.1) [Knowledge]

**2.** Apply De-Morgan’s theorem to [2M] (C.O.No.2) [Application]

**3.** Define ‘min term’ and ‘max term’. [2M] (C.O.No.1) [Knowledge]

**4.** Draw the OR logic using only NAND gates. [2M] (C.O.No.1) [Knowledge]

**5.** What is a don't care condition? [2M] (C.O.No.1) [Knowledge]

**6.** How logic circuits of a digital system are classified? [2M] (C.O.No.1) [Knowledge]

**7.** Define Half adder and Full adder. [2M] (C.O.No.2) [Application]

**8.** What is combinational circuit? Give examples. [2M] (C.O.No.2) [Application]

**9.** Write an expression for borrow and difference in a full subtractor circuit

[2M] (C.O.No.2) [Application]

**10.** How many selection lines are needed for 8:1 Multiplexer? [2M] (C.O.No.2) [Application]

**Part B [Thought Provoking Questions]**

**Answer all the Questions. Each question carries five marks. (4Qx5M=20M)**

1. Given Y (A, B, C, D) = Σm (0,1,3,9) draw the K-map and obtain the simplified expression. Realize the minimum expression using basic gates. [5 Marks] (C.O.No.2) [Application]
2. Implement the XOR using NAND and NOR universal gates. [5 Marks] (C.O.No.1) [Knowledge]
3. Design and implement full adder using two half adders. [5 Marks] (C.O.No.3) [Application]
4. Use a multiplexer having 3 data select lines to implement the logic for the function

f(A, B, C, D)= Σm (0,1,2,3,4,10,11,14,15) [5 Marks] (C.O.No.3) [Application]

**Part C [Problem Solving Questions]**

**Answer all the Questions. Each question carries twenty marks. (3Qx20M=60M)**

**15.** The D flip-flop is a special case of SR flip-flop. The D flip-flop can be either positive edge triggered or negative edge triggered. Draw the logic symbol, logic diagram, write the truth table, characteristic table and characteristic equation of a positive edge triggered D flip-flop.

[20M] (C.O.No. 4) [Application]

**16.** A flip-flop is a sequential digital logic circuit and is used to design counters. The JK flip-flop full form is Jack Kilby flip-flop. The JK flip-flop can be built using universal gates such as NAND gates. Design a 3-bit down counter using JK flip-flop. [20M] (C.O.No. 5) [Application]

**17.** A flip-flop is a sequential digital logic circuit and is used to design counters. The SR flip-flop full form is Set Reset flip-flop. The SR flip-flop can be built using universal gates such as NAND gates. Design a 3-bit up counter using SR flip-flop. [20M] (C.O.No. 5) [Application]