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PRESIDENCY UNIVERSITY BENGALURU

 SCHOOL OF INFORMATION SCIENCE

MAKE UP EXAMINATION - JULY 2024

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| **Semester : II** | **Date :03/July/2024** |
| **Course Code :ECE2006** | **Time :** **01.30pm to 04.30pm** |
| **Course Name :DIGITAL ELECTRONICS** | **Max Marks :100** |
| **Program :B.Tech.,** | **Weightage :50%** |

**Instructions:**

1. *Read all questions carefully and answer accordingly.*
2. *Question paper consists of 3 parts.*
3. *Scientific and non-programmable calculator are permitted.*
4. *Do not write any information on the question paper other than Roll Number.*

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| **PART A** |
|  **ANSWER ANY 5 QUESTIONS 5Q X 2M=10M** |
| 1 | Find the equivalent Binary and Octal Number for the given Decimal value 42145 : | (CO 1) | [Knowledge] |
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| 2 | Convert the following Boolean expression Y=P+QR′+PQ+P′QR into canonical SoP form? | (CO 2) | [Knowledge] |
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| 3 | Write the difference between a combinational logic circuit and a sequential logic circuit? | (CO 2) | [Knowledge] |
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| 4 | In a Priority Encoder, D0, D1 & D2 are high means what is the encoded value of an 8 into 3 line Encoder? | (CO 3) | [Knowledge] |
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| 5 | Given the Boolean expression is f= P'Q+ PQ'+PQ. How many minimum number of two input NAND gates are required to implement the given Boolean expression? | (CO 2) | [Knowledge] |
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| 6 | Draw the OR gate logic using NAND gate: | (CO 1) | [Knowledge] |
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| 7 | Draw the 2x1 Multiplexers using basic gates: | (CO 3) | [Knowledge] |

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| **PART B** |
|  **ANSWER ANY 5 QUESTIONS 5Q X 10M=50M** |
| 8 | Raj is an engineering student. In his mini project, he has to design a circuit which has three inputs A, B, Cin and Two outputs. The circuit performing the summations of all input and produce sum and carry output. But Raj has only 3 into 8 line Decoder IC. Give the truth table and circuit diagram for his project with available Decoder:  | (CO3) | [Application]. |
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| 9 | Design a COUNTER for Initial state is 000 and final state is 111, after getting final state, the circuit should start counting over from initial state (3 bit UP counter). You are provided with JK flip flop and all possible basic gates with working conditions. Through the state table and K map simplification, design a circuit for the specification.  | (CO4) | [Application]. |
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| 10 | A engineering student during his mini project, he has to design a circuit which has three inputs A, B, C and Two outputs. The circuit performing the operations of Full Subtractor. But Rahim has only two number of Half Subtractor integrated circuit and OR gate. Guide him to design the Full Subtractor by using Half Subtractor.  | (CO3) | [Application]. |
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| 11 | Design a digital logic function which is described by the following Boolean Function in SoP, F(A,B,C,D)=⅀(1,3,4,11,12,13,14,15). using only 8x1 MUX.  | (CO3) | [Application]. |
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| 12 | Design a combinational logic circuit using basic gates only, which consider the three values namely minuend, subtrahend, and borrow-in to generate the difference and borrow outputs. | (CO3) | [Application]. |
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| 13 | Convert a **D flip-flop** into **JK flip-flop** and write the Characteristic table of both:  | (CO4) | [Application]. |
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| 14 | Using K-map method, Simplify the given function (minimum SOP)  F(A,B,C,D) =A'B'C'D' +AC'D'+ B'CD'+ A'BCD +BC'D | (CO2) | [Application]. |
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| **PART C** |
|  **ANSWER ANY 2 QUESTIONS 2Q X 20M=40M** |
| 14 | Using K-map method, Simplify the given function (minimum SOP) and realize using only NAND gate **F=∑m(0,2,3,6,7) + d(8,10,11,15**) | (CO2) | [Application]. |
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| 15 | A student wants to design a digital logic switching function which is described by F(W,X,Y,Z)=πM(0,2,5,7,8,10). But he has only Two input and Three input NAND gates. Guide the students to derive and implement the circuit. | (CO2) | [Application]. |
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| 16 | A sequential circuit has two JK flip flop A and B, which is described by the following flip flop input equation. JA= B KA=Bx’JB=x’ KB=Ax’+B’x Where x is the external input, A and B are the present state of flip flop. Derive the Sequential Logic Circuit  | (CO4) | [Application]. |
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